Synopsys' New DesignWare DDR Explorer Tool Delivers Up to 20 Percent Improvement in DDR Memory Subsystem Efficiency

Performance Analysis Tool Accelerates Optimization of Address Mapping, Clock Frequency and Quality of Service for DesignWare DDR Memory Controller

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Highlights:

- DesignWare DDR Explorer enables designers to optimize memory subsystems for power, performance and cost through a graphical simulation and analysis environment
- Explore and adjust Synopsys' DesignWare DDR Memory Controller configurations to achieve up to 20 percent improvement in memory bandwidth
- Optimize address mapping, clock frequency and quality of service to select lower cost, lower power DRAM memories
- Achieve 10X faster turnaround time compared to RTL analysis with transaction-level simulation to visualize performance and conduct performance sensitivity analysis

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the new DesignWare® DDR Explorer performance analysis tool, which enables designers to quickly optimize Synopsys' DesignWare Enhanced Universal DDR Memory Controller (uMCTL2) for performance, power and cost. Using DDR Explorer, designers can analyze their DDR memory subsystem and optimize their architecture to increase efficiency by up to 20 percent, while achieving 10X faster turnaround time compared to RTL analysis. With the graphical simulation and analysis provided by DDR Explorer, designers can quickly select the right memory type for the lowest bill of material (BOM) cost and system power. DDR Explorer supports all of the industry standard DRAM interfaces for mobile and enterprise applications, including LPDDR2, LPDDR3, DDR2, DDR3 and DDR4.

DDR Explorer integrates a transaction-level architecture model of the DesignWare DDR Enhanced Universal Memory Controller with a graphical simulation and analysis environment that enables designers to define, run and analyze hundreds of scenarios to identify the best memory controller configuration. RTL-based performance checking, while required for final validation, typically has longer turnaround times and limits the practical number of design explorations during a project to fewer than 25. DDR Explorer enables thorough performance and power sensitivity analysis for over 250 simulations in the same amount of time. By identifying heavy traffic conditions and bottlenecks, designers can explore the DDR memory controller parameter configurations and register settings to optimize the DDR memory performance. This results in up to 20 percent greater memory efficiency, lower power consumption and lower memory cost, without sacrificing other memory performance requirements. The optimized configuration from DDR Explorer is used for DDR memory controller RTL IP configuration and performance validation, speeding the implementation and verification of the IP.

"With DDR Explorer, designers can rapidly configure, simulate and analyze the DDR memory controller and PHY subsystem," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "DDR Explorer enables designers to significantly reduce the effort of integrating DesignWare DDR Enhanced Universal Memory Controller and PHY IP into their SoCs for faster time-to-market."

Availability & Resources

DesignWare DDR Explorer is available now.

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  - Learn more about DesignWare DDR Explorer at: http://www.synopsys.com/dw/ipdir.php?ds=dwc_ddr_explorer

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, analog IP, complete interface IP solutions consisting of controller, PHY and next-generation verification IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and customized IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit https://www.synopsys.com/designware

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at https://www.synopsys.com.

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