Synopsys Expands Memory Verification IP Portfolio with UFS, UniPro and eMMC to Accelerate Verification Closure for Mobile Designs

MOUNTAIN VIEW, Calif., Jan. 21, 2015 /PRNewswire/ -- Synopsys, Inc. (NASDAQ: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the expansion of its memory Verification IP (VIP) portfolio to include key titles for the mobile industry. Synopsys memory VIP is based on a native SystemVerilog architecture to enable enhanced ease of use, integration and configurability. With these advanced features, project teams using the JEDEC UFS, MIPI® UniPro℠ and JEDEC eMMC protocols can further accelerate verification closure of mobile block, subsystem and system-on-chip (SoC) designs.

"The adoption of M-PHY® and UniPro into JEDEC's UFS memory interface provides lower power and higher performance and enables the industry to stay on the leading edge of the performance curve," said Joel Huloux, chairman of MIPI Alliance. "Synopsys' feature-rich VIP and test suites with built-in coverage for the UFS, UniPro and M-PHY specifications strengthen the ecosystem required to enable fast development of mobile and mobile-related products, and it enables higher-confidence compliance verification."

VIP for the emerging UFS and UniPro protocols also includes self-contained compliance test suites to accelerate verification closure and eliminate the tasks of developing a verification environment and tests. The test suites are delivered as native SystemVerilog source code for improved reuse, extensibility and debug. The JEDEC eMMC VIP includes support for eMMC Card and Host. All verification IP and test suites are based on a consistent SystemVerilog UVM architecture to enable easy adoption.

Synopsys' broad portfolio of bus, interface and memory VIP includes built-in coverage and verification plans to enable coverage closure. It also includes support for Verdi® Protocol Analyzer to provide protocol-aware debug. Synopsys VIP for the JEDEC UFS, MIPI UniPro and JEDEC eMMC memory protocol specifications provides a comprehensive set of protocol, methodology, verification and productivity features, enabling users to achieve rapid verification convergence.

"We have worked closely with our customers and the standards boards to provide verification IP for the latest protocols, including technology to enable fast deployment of VIP into verification environments and to rapidly achieve verification closure," said Debashis Chowdhury, vice president of R&D for the Synopsys Verification Group. "The mobile market segment is extremely competitive, with designers at all levels of the product hierarchy continually striving to achieve more performance with increased functionality at the lowest levels of power consumption and cost. On-time availability of emerging protocols and the latest versions of current protocols enable designers to achieve their verification goals and hit project schedules."

Availability

Synopsys Verification IP for UFS, MIPI UniPro and eMMC are available standalone today and as part of the Synopsys VIP Library as well as in the Verification Compiler™ product. The Synopsys DesignWare® digital controllers for UFS, MIPI UniPro and eMMC are also available now.

About Synopsys Verification IP

Synopsys VIP, based on its next-generation architecture and implemented in native SystemVerilog, offers native performance, native debug with Verdi, enhanced VIP ease of use, configurability, coverage and source code compliance test suites. These capabilities substantially increase user productivity for one of the most difficult and time-consuming aspects of SoC design and verification. Synopsys VIP Library includes a broad portfolio of interface, bus, and memory protocols. More information is available at www.synopsys.com/vip.

About Synopsys

Synopsys, Inc. (NASDAQ:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.

650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 x115
lgmartin@mcapr.com