Synopsys' PrimeTime ADV Achieves Rapid Adoption for Fastest Timing Closure

Adopted by More than 70 Semiconductor Companies with Over 50 Tapeouts in First 9 Months

MOUNTAIN VIEW, Calif., Dec. 17, 2014 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced its PrimeTime® ADV advanced timing closure and signoff solution has been adopted by more than 70 leading semiconductor companies and enabled more than 50 successful tapeouts in just nine months since it became generally available. The key to its rapid adoption is ease of integration into existing timing closure flows, fast turnaround time and the ability to significantly reduce the number of timing ECO (engineering change order) iterations on designs across a broad range of applications and process nodes. Companies that have deployed PrimeTime ADV include Achronix Semiconductor, All Winner Technology, GUC, Infineon Technologies, Renesas, Samsung, STMicroelectronics, Toshiba and others.

Timing closure is one of the biggest challenges highlighted by chip designers, often encompassing 30 percent of the physical implementation design schedule.

"Achronix is focused on achieving maximum clock speeds for our next generation 14 nanometer FPGAs. Having the best-in-class development tools is critical for us to increase our competitive advantage beyond our current and highly successful 22-nanometer Speedster22i FPGA products," said Chris Pelosi, director of engineering at Achronix Semiconductor. "With Synopsys' PrimeTime ADV tool as part of our development kit, our designers can achieve our high frequency targets and cut the design cycle time."

Traditional ECO solutions are no longer scaling to the complexity of timing closure and the pressure to improve performance and reduce power and area at emerging and established technology nodes. Further, highly dense designs in terms of routing and cell placement resources make development of ECO solutions costly. Hence, designers are looking to move away from traditional ECO solutions to more intelligent solutions to speed-up the ECO schedule by 2X.

To address this challenge, PrimeTime ADV provides a physically aware timing and power recovery solution built on the trusted PrimeTime signoff timing engine. This enables signoff quality timing which comprehends global timing effects like splitting parasitics, crosstalk impact and on-chip-variation (OCV), something existing commercial add-on ECO solutions lack. Signoff correlation, essential for faster timing closure, is deficient in non-signoff timing tools, a situation which leads to costly ECO iterations. PrimeTime ADV's signoff-driven ECO guidance, when tightly integrated with Synopsys' leading StarRC™ extraction solution and IC Compiler™ physical implementation solution, delivers the best single-pass results using innovative techniques such as on-route-buffering. With the recent PrimeTime ADV release, leakage recovery has been extended to total power recovery, assisting the mobile and consumer designs to further reduce their total power.

"Delivering automated solutions that enable our customers to achieve time-critical and aggressive timing and power goals with confidence is a major focus at Synopsys," said Antun Domic, executive vice president and general manager of Synopsys' Design Group. "PrimeTime ADV's plug-n-play ECO solution, tightly coupled with StarRC and IC Compiler, helped our customers quickly adopt and deploy this technology in their timing closure flow."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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