Synopsys' New LPDDR4 Verification IP Accelerates Verification Closure for High-Performance Low Power Designs

Native SystemVerilog-based Memory VIP Portfolio Expanded to Support JEDEC LPDDR4 with Built-in Coverage, Verification Plan and Protocol-aware Debug

MOUNTAIN VIEW, Calif., Dec. 9, 2014 /PRNewswire/ -- Synopsys, Inc. (NASDAQ: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the immediate availability of verification IP (VIP) for LPDDR4. Synopsys VIP for LPDDR4 is based on a 100 percent native SystemVerilog Universal Verification Methodology (UVM) architecture to enable ease of use, ease of integration and performance. Complete with verification plans, built-in coverage and a protocol-aware memory debug environment, Verdi® Protocol Analyzer, Synopsys VIP for LPDDR4 is a complete VIP solution that accelerates verification closure for designers of low power memory controllers and systems on chips (SoCs).

"LPDDR4 is an exciting step forward in technology providing lower power and higher performance, enabling the mobile industry to stay on the leading edge of the performance curve," said Kevin Widmer, vice president of technical marketing at SK hynix. "The release of Synopsys memory VIP with advanced verification features devised for the LPDDR4 specification enables faster development of products and enables higher-confidence in compliance verification for SoCs and designs with memory interfaces."

Synopsys' 100 percent native SystemVerilog VIP for the JEDEC LPDDR4 memory protocol specification includes transactor and monitor functions to provide a comprehensive set of protocol, methodology, verification and productivity features, enabling users to achieve rapid verification convergence on LPDDR4-based designs. In addition to providing LPDDR protocol verification, the Synopsys LPDDR4 VIP can be dynamically configured to model any memory vendor component without the need to recompile, enabling SoC teams to rapidly verify the range of components that will be used with their SoCs.

"We have collaborated extensively with leading-edge SoC design teams to address the increasingly demanding process of protocol compliance for on-chip buses, off-chip interfaces and memory," said Debashis Chowdhury, vice president of R&D for the Synopsys Verification Group. "We continue to deliver solutions that enable designers to accelerate their SoC verification closure and decrease time to market. Synopsys LPDDR4 VIP provides SoC teams with the built-in protocol knowledge, features and methodology support to save time, increase design quality and meet project schedules."

Availability

Synopsys VIP for LPDDR4 is available today standalone and as part of the Synopsys VIP Library and the Verification Compiler product. LPDDR4 VIP is also included as part of Synopsys' complete DesignWare® IP solution for LPDDR4 that includes controllers, PHY and Verification IP.

About Synopsys Verification IP

Synopsys VIP, based on its next-generation architecture and implemented in native SystemVerilog, offers native performance, native debug with Verdi, enhanced VIP ease of use, configurability, coverage and source code compliance test suites. These capabilities substantially increase user productivity for one of the most difficult and time-consuming aspects of SoC design and verification. Synopsys' VIP library includes a broad portfolio of interface, bus and memory protocols.

More information is available at www.synopsys.com/vip.

About Synopsys

Synopsys, Inc. (NASDAQ:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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