Oticon Standardizes on Synopsys' Design Compiler Graphical

Reduced Congestion and MCMM Synthesis Cut Weeks from Schedule

MOUNTAIN VIEW, Calif., Nov. 18, 2014 /PRNewswire/ --

Highlights:

- Oticon has widely deployed Design Compiler Graphical for implementation of its hearing solutions ICs
- Multi-corner multi-mode (MCMM) synthesis results in lower leakage and faster convergence
- Congestion reduction in Design Compiler Graphical enables Oticon to achieve faster design performance within shorter schedules

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that Oticon, Inc., a leading manufacturer of hearing solutions, has deployed Synopsys' Design Compiler® Graphical RTL synthesis solution for implementing all of its hearing solutions ICs. Minimizing IC area and power consumption while maximizing functionality and performance are key factors in delivering the smallest hearing aids with the best voice quality and feature set. To achieve these goals, Oticon has widely deployed Design Compiler Graphical's congestion optimizations and MCMM synthesis technologies and is realizing lower leakage, faster design performance and a highly convergent design flow, shortening schedules by weeks.

"Meeting aggressive power and area budgets within tight schedules is of primary importance for hearing solutions ICs," said Mogens Isager, lead developer, Physical IC Design at Oticon, Inc. "With Design Compiler Graphical's advanced congestion and MCMM optimizations, we are seeing 20 percent less congestion in high-density cell areas, improved design frequency, lower leakage power and faster place-and-route runtimes, which enable us to meet all our design goals and save a few weeks of schedule. Design Compiler Graphical is now a standard component of our design flow."

Design Compiler Graphical addresses challenging design requirements at both established and emerging process nodes. It provides designers with visualization of congested circuit regions and allows them to perform specialized synthesis optimizations to minimize congestion in these areas. Additionally, new optimization technologies monotonically reduce design area and leakage power by an average of 15 percent while maintaining timing quality of results (QoR).

These capabilities in conjunction with MCMM synthesis and shared physical technologies with Synopsys' IC Compiler™ place and route solution enable customers to achieve the best timing, area, power and routability QoR, reduce design iterations and deliver their products to market faster.

"Market leaders, such as Oticon, who differentiate their products by minimizing power and area while maximizing performance, rely on Design Compiler Graphical to achieve aggressive design objectives within tight schedules," said Bijan Kiani, vice president of marketing in Synopsys' Design Group. "Design Compiler Graphical's innovative synthesis technologies and tight links with the Galaxy™ Design Platform enable our customers to accelerate delivery of industry-leading products to their target markets."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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