Synopsys Announces Availability of DesignWare Non-Volatile Memory IP for TowerJazz 180-nm Process Technology

Silicon-Proven, Reprogrammable NVM IP Delivers Smallest Area for Calibration and Trimming Applications

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Highlights:

- Reprogrammable NVM IP on TowerJazz 180-nm process technology enables analog IC trimming and in-field calibration without additional masks or process steps
- Small footprint reprogrammable NVM IP integrates charge pump, digital controller and oscillator to reduce overall IC area
- Operates from a single core supply to reduce system design complexity

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of the silicon-proven DesignWare® AEON® Few Time Programmable (FTP) Trim Non-Volatile Memory (NVM) IP for TowerJazz 180-nanometer (nm) SL process technology. The NVM IP integrates high voltage generation and control circuitry using a standard CMOS technology without the need for additional masks or processing steps. The IP operates from a single core supply, eliminating the complication of providing a separate voltage for NVM programming. The DesignWare AEON FTP Trim NVM IP provides the smallest area for precision analog IC trimming and sensor calibration applications, in a similar footprint as one-time programmable (OTP) solutions with the advantage of reprogrammability.

"It is critical for us to collaborate with an established IP provider who understands our technology needs and is able to deliver high-quality and feature-rich IP solutions quickly," said Soonwon Hong, vice president of Leading Division at TLi. "Integrating Synopsys' proven DesignWare AEON FTP Trim NVM IP for the TowerJazz 180-nanometer process technology delivered the area and performance we required, while reducing integration risk and accelerating our time-to-market by three months."

"Synopsys DesignWare AEON FTP Trim NVM IP enabled us to meet our customers' aggressive schedule requirements and need for small reprogrammable non-volatile memory IP in the TowerJazz 180-nanometer process technology," said Tal Bar (Dotan), director of IP Design Services at TowerJazz. "The combination of Synopsys' trusted IP solution and TowerJazz's IC manufacturing capabilities helps our mutual customers achieve their design goals faster and with less integration risk."

The reprogrammability advantage of the NVM IP enables designers to make in-field calibration updates, which allow end customers to make customizations and changes. The NVM IP includes necessary support and control circuitry including all high voltage generation and distribution required for programming to reduce system design complexity and IC area. It also supports up to 1 k bit instances, up to 10,000 write cycles, and more than 10 years of data retention at a temperature range (-40 degrees C to +125 degrees C) for industrial applications.

"As a leading provider of reprogrammable NVM IP, Synopsys delivers high-quality solutions that enable designers to incorporate the required functionality into their SoCs with less risk," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "With more than four billion customer ICs shipping with DesignWare NVM IP to-date, Synopsys delivers a silicon-proven, fully qualified NVM IP solution for TowerJazz 180-nanometer process technology that helps designers meet their project schedule and accelerate their time to volume."

Availability

The DesignWare AEON Trim NVM IP for TowerJazz 180-nm process is available now. DesignWare NVM IP is also available for multiple other foundries in 250-nm to 40-nm process technologies.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controller, PHY and next-generation verification IP, analog IP, embedded memories, logic libraries, processor solutions and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and customized IP subsystems for rapid

integration of IP into SoCs. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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