Synopsys' New USB 3.1 IP Solution Enables 10 Gbps Data Transfer Speeds for Storage, Digital Office and Mobile Applications

Industry-First Solution Includes DesignWare USB 3.1 Controller, IP Virtual Development Kit and Verification IP

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Highlights:

- High-quality DesignWare USB 3.1 Device Controller IP reduces integration risk and accelerates availability of USB 3.1 SoCs
- USB 3.1 IP integrators can gain 2X faster data transfer speeds than USB 3.0 and upgrade to USB 3.1 IP with no changes to existing USB software
- DesignWare USB 3.1 IP Virtual Development Kit helps developers quickly bring-up, enhance and optimize existing software
- Verification IP, written in native SystemVerilog UVM, provides thorough built-in coverage, verification plan and debug to simplify testbench development
- HAPS FPGA-based prototyping system enables hardware/software integration and system validation of USB 3.1 designs

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today introduced the industry's first USB 3.1 IP solution, consisting of DesignWare® USB 3.1 Device Controller, an IP Virtual Development Kit (VDK) and verification IP (VIP) to accelerate the development of high-performance storage, digital office and mobile system-on-chip (SoC) applications. Synopsys' DesignWare USB 3.1 IP solutions support 10 Gbps data transfer rates, power-down capabilities and compatibility with existing USB 3.0 software stacks and device protocols. Based on the DesignWare USB 3.0 Controller IP architecture, which has shipped in more than 100 million SoCs, the DesignWare USB 3.1 Device Controller IP enables designers to integrate USB 3.1 functionality with significantly less risk and faster time-to-market.

"Mobile, storage and digital office applications that will take advantage of USB 3.1's 10 Gbps performance are in development now," said Terry Moore, CEO at MCCI. "Designers facing tight schedules can save up to twenty months of engineering effort by using their existing DesignWare USB 3.0 software or, if changing controllers or operating systems, by using MCCI's pre-tested off-the-shelf Datapump USB device stack."

"As an active member of the USB-IF for more than 18 years, Synopsys continues to develop IP products that ease the integration and adoption of the latest USB specifications," said Jeff Ravencraft, USB-IF president and COO. "Initial USB 3.1 products are expected to appear in early 2015 and the availability of integration-ready USB 3.1 IP is critical. Companies like Synopsys give designers the ability to more easily incorporate the USB 3.1 interface into their SoCs, pushing USB performance ever higher."

The DesignWare USB 3.1 IP VDK, part of the Synopsys IP Accelerated initiative, helps developers quickly bring-up, enhance and optimize existing software for their specific DesignWare USB 3.1 Device Controller configuration. The IP VDK consists of a reference virtual prototype that includes a processor subsystem reference design, a configurable model of the DesignWare USB 3.1 Controller IP, a Linux® software stack and reference drivers. Software developers can use the IP VDK as a proven target for early software development, bring-up, debug and test in parallel with SoC development. Hardware developers can use the HAPS® FPGA-based prototyping system for hardware/software integration and system validation of USB 3.1 designs, as demonstrated in November 2013.

Synopsys' USB 3.1 VIP is based on Synopsys' native SystemVerilog and native UVM architecture, offering ease of integration, high performance, configurability, coverage and debug to speed the protocol verification process. The USB 3.1 VIP supports Verdi Protocol Analyzer, a protocol-centric debug environment that substantially increases user productivity with protocol-aware features to simplify viewing and debug of complex protocols.

"As a leading provider of USB IP for more than a decade, Synopsys provides the high-quality IP designers need to meet their evolving power, performance and area requirements," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "With our extensive knowledge in developing USB IP, more than 3,000 USB design wins and billions of SoCs shipped with DesignWare USB IP, designers know they can rely on Synopsys when integrating the latest USB functionality into their SoCs."

Availability

The DesignWare USB 3.1 Device Controller IP and USB 3.1 VIP are available now. The DesignWare USB 3.1 IP Virtual Development Kit is planned to be available in Q1 2015.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controller, PHY and next-generation verification IP, analog IP, embedded memories, logic libraries, processor solutions and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and customized IP subsystems for rapid integration of IP into SoCs. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934 regarding the expected release and benefits of the DesignWare ARC HS38 Processor. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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