Synopsys IC Compiler II Delivers Five Fold Implementation Speed up, Enables Silicon Success

Success Drives Panasonic SoC Adoption of IC Compiler II

MOUNTAIN VIEW, Calif., Oct. 28, 2014 /PRNewswire/ --

Highlights

- IC Compiler II enables first-time working silicon for high-performance multimedia design in 40-nm technology
- 5X faster design implementation enables faster turn-around-time for large partitions
- Ability to seamlessly handle more modes and corners drastically improves signoff convergence and reduces ECO iterations

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that its IC Complier™ II place-and-route tool enabled Panasonic Corporation System LSI Business Division (Panasonic SoC) to achieve silicon success with their high-end multimedia chip. Unveiled at Synopsys User Group (SNUG) in Silicon Valley earlier this year, IC Compiler II is a game-changing successor to the IC Compiler™ product, the industry's current leading place-and-route solution for advanced designs at both established and emerging nodes. Key capabilities in IC Compiler II include rapid design exploration, unique new clock-building, analytics-driven optimization to boost quality-of-results and extensive use of multi-mode and multi-corner optimization throughout the flow to accelerate turnaround time. The unique benefits it offered with five times faster implementation, IC Compiler II is now seeing expanded use to other designs at 40 nanometer (nm) and 28 nm process technology nodes.

"IC Compiler II was instrumental in enabling us to hit our market window and achieve silicon success for our complex multimedia chip. We are now entering volume production," said Hiroki Tomoshige, general manager at Panasonic Corporation System LSI Business Division, Division 3, Second Development Group. "We are very pleased with the breakthrough performance IC Compiler II has delivered to shorten our design cycles and get our competitive products to market faster."

IC Compiler II was built from the ground up to deliver a major leap forward in physical design productivity. Based on a new multi-everything infrastructure and multicore technology that enables ultra-high-capacity design planning capability, unique clocking technology and advanced global and analytical closure techniques, IC Compiler II delivers a groundbreaking 10-times increase in design throughput. IC Complier II's "analytically-global" optimization provides faster, broader and more convergent physical synthesis and closure. This natively multi-threaded technique utilizes new, highly scalable timing and extraction engines that enable extensive multi-corner and multi-mode (MCMM) optimization. Early and broad analysis enables optimization for large number of concurrent scenarios, improving signoff convergence and reducing ECO iterations to a minimum. Additionally, patent-pending MCMM-aware local-skew clock construction techniques enable significant speed up in the building of complex clock networks with hundreds of domains and achieve the high-frequency clock requirements that are typical for the success of high-end chips.

"The unique benefits it offers with five times faster implementation illustrates why our customers are seeing IC Compiler II as a game-changing solution that is redefining the implementation landscape," said Antun Domic, executive vice-president and general manager of the Design Group at Synopsys. "We are engaged broadly to bring the power of 10X delivered by IC Compiler II to more customers and help them get more competitive products to market faster."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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