Synopsys STAR Memory System Multi-Memory Bus Processor Enables 10 Percent Die Size Reduction for Marvell SoC

New Multi-Memory Bus Processor Cuts Test Logic in Half While Maintaining High Performance for Networking SoC

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Highlights:

- Marvell achieved silicon success for networking SoC using the multi-memory bus (MMB) processor in the Synopsys DesignWare STAR Memory System for embedded test and repair
- Reduced area and power with a single MMB processor providing common test and repair logic for all memory instances mapped to a shared bus
- Decoupled embedded test and repair logic from the performance- and area-critical block under test by placing MMB processor outside the block
- Achieved high test coverage with comprehensive automated test and repair solution for embedded memory arrays
- Accelerated test pattern development and silicon bring-up

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that Marvell Semiconductor, Inc. used Synopsys' DesignWare® STAR Memory System's new multi-memory bus (MMB) processor to achieve a 10 percent reduction in total die size while maintaining product quality and performance for its networking system-on-chip (SoC). Using the DesignWare STAR Memory System embedded test and repair solution, Marvell accelerated silicon bring-up and achieved silicon success.

Marvell's design includes hundreds of memory instances and required a test solution that would minimize area and routing congestion without affecting performance or quality. The MMB processor in the DesignWare STAR Memory System contains all of the logic needed to implement a comprehensive test and repair strategy for all memory instances mapped on a multi-memory test bus. Marvell was able to use a single MMB processor to test hundreds of memories, saving over 50 percent in memory test logic area.

With the addition of the MMB processor to the STAR Memory System, designers now have the flexibility to either decouple test logic from the block under test or optimally place the test logic within the block to minimize the impact on performance and area. The MMB processor is ideally suited for high-performance design blocks and processor subsystems with L1 and L2 caches optimized for maximum performance.

"Using the DesignWare STAR Memory System has significantly reduced our silicon area and cost," said Sohail Syed, senior director of Engineering at Marvell. "We were able to not only reduce total die size by 10 percent, but also meet our stringent product quality goals and high performance requirements by using the new MMB processor. In addition, the STAR Memory System's Yield Accelerator and Silicon Browser tools have significantly improved our silicon bring-up efforts by making test pattern development and validation more efficient."

The DesignWare STAR Memory System is an automated pre- and post-silicon memory test, diagnostic and repair solution that enables designers to implement high test coverage, reduce design time, lower manufacturing test costs and maximize manufacturing yield. Synopsys employs rigorous simulation and silicon characterization methods to identify prevalent memory defect mechanisms at every process node and then develops the test algorithms to detect them. Used in billions of chips, the STAR Memory System is a two-time winner of *Test & Measurement World's* prestigious "Best in Test" Award.

"Synopsys provides robust test solutions that enable designers to meet their challenging performance, power and area requirements without compromising on quality," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "With the addition of the MMB processor in the DesignWare STAR Memory System, designers can reduce their on-die test footprint and maintain high performance while implementing comprehensive memory test solutions for faster time to volume."

Availability

The DesignWare STAR Memory System with MMB processor is available now.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controller, PHY and next-generation verification IP, analog IP, embedded memories, logic libraries, processor solutions and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and customized IP subsystems for rapid integration of IP into SoCs. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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