SMIC Certifies Synopsys IC Validator for Signoff Physical Verification

28-nm Runset Availability Enables Signoff Physical Verification for Mutual Customers

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Highlights:

- Fully qualified 28-nm signoff physical verification runsets are available from SMIC for DRC, LVS and metal fill
- Certified runsets enable SMIC and Synopsys' mutual customers to leverage IC Validator In-Design physical verification and transistor-level parasitic extraction with StarRC
- Ongoing collaboration targets expanded coverage for SMIC's process technologies, providing mutual customers more options

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that its IC Validator product has been certified by Semiconductor Manufacturing International Corporation (SMIC) for signoff physical verification of their 28-nanometer (nm) PolySiON (PS) manufacturing process. This availability gives mutual customers access to a wider selection of leading signoff tools for physical verification. The fully qualified design rule checking (DRC) and layout-versus-schematic (LVS) runsets are available for download from the SMIC website at www.smics.com.

"Formalizing our certification of IC Validator is a big step forward in supporting a number of our mutual customers for signoff verification. We are expanding our 28-nm pilot production through the end of 2014," said Dr. Waisum Wong, senior director of Technology Development at SMIC. "We expect that the 28-nm product life cycle longevity will exceed previous nodes, and we are pleased to include IC Validator as part of our signoff infrastructure."

IC Validator, part of the Synopsys Galaxy™ Design Platform, is a comprehensive solution for all physical verification tasks, including DRC, LVS, manufacturability enhancement, electrical rule checking (ERC) and metal fill insertion. Its modern architecture and excellent multi-core scalability make IC Validator the signoff tool of choice for a growing number of customers who are working on small analog designs, or large digital system-on-chip (SoC) designs. Foundry-certified runsets enable Synopsys' In-Design physical verification with IC Compiler™ place and route and StarRC™ transistor-level parasitic extraction. IC Validator enables coding at higher levels of abstraction, which allows SMIC to streamline design rule development and deployment, and provide mutual customers with the high accuracy and excellent scalability needed for designs done on leading-edge process nodes.

"As manufacturing complexity places increased pressure on designers to deliver within tighter schedules, it is important that we continue to collaborate closely with foundries like SMIC," said Antun Domic, executive vice president and general manager of the Design Group at Synopsys. "SMIC's certification demonstrates how designers with the most demanding designs are driving the market towards better signoff verification solutions that are also closely integrated into their design flows."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com

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