VIA Technologies Cuts Silicon Test Time by 11X Using Synopsys' DFTMAX Ultra

Standardizes on DFTMAX Ultra for Designs with Few Test Pins

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Highlights:

- DFTMAX™ Ultra compression technology deliver 11X higher compression and reduced test time
- Higher test quality with shorter test time drove VIA's standardization on DFTMAX Ultra for pin-limited designs
- Deployment of DFTMAX Ultra, built into Synopsys' Design Compiler® RTL Synthesis solution, was done within a week

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that VIA Technologies, the foremost fabless supplier of power efficient x86 processor platforms, successfully taped out a system-on-chip (SoC) design using Synopsys' DFTMAX Ultra compression, meeting test time and quality goals. The need to shorten test time in conjunction with increasing design complexity drove VIA Technologies requirement for higher test compression. DFTMAX Ultra and Synopsys' TetraMAX® ATPG delivered 11X higher compression while maintaining high test quality and requiring only one week to deploy. As a result, VIA Technologies has standardized on DFTMAX Ultra and TetraMAX for all pin-limited designs.

"DFTMAX Ultra delivered 11X higher compression on our pin-limited design, which allowed us to meet our manufacturing test goals," said JC Chen, design service manager of the Hardware Technology Development Center at VIA Technologies. "We were able to incorporate DFTMAX Ultra into our design flows within a few days without impacting our stringent schedules. Due to the superior results DFTMAX Ultra delivers, we will be using it for all our pin-limited designs."

Design teams are under pressure to ensure high manufacturing defect coverage while facing multiple factors that reduce the number of pins available for test. These include designs such as mobile applications that are pin-limited, large SoCs that have few pins per core for test access, as well as a technique known as multisite testing that checks for defects across multiple dies simultaneously. Companies like VIA Technologies are deploying DFTMAX Ultra to address the increased costs typically associated with pin-limited testing. By achieving significantly higher compression than previous technologies, DFTMAX Ultra enables high defect coverage utilizing as few as one pair of test pins. Built into Design Compiler, DFTMAX Ultra synthesizes the test compression logic into a design, then sets up Synopsys TetraMAX ATPG to generate high defect-coverage, power-aware test programs.

"A growing number of semiconductor companies, such as VIA Technologies, are adopting DFTMAX Ultra to aggressively cut test time and maintain high test quality," said Bijan Kiani, vice president of marketing for Synopsys' Design Group. "With innovative compression technology and value links to other products in the Synopsys Galaxy™ Design Platform, DFTMAX Ultra is helping our customers meet their most challenging design and test goals faster."

About the Synopsys Synthesis-Based Test Solution

The Synopsys synthesis-based test solution is comprised of DFTMAX™ Ultra, DFTMAX and TetraMAX for power-aware logic test and physical diagnostics; the DesignWare® STAR Hierarchical System for hierarchical test of IP and cores on an SoC; the DesignWare STAR Memory System® for embedded test, repair and diagnostics; Yield Explorer® tool for design-centric yield analysis; and the Camelot™ software system for CAD navigation. Synopsys' test solution combines Design Compiler RTL synthesis with embedded test technology to optimize timing, power, area and congestion for test as well as functional logic, leading to faster time-to-results due to zero or minimal design iterations. The solution contains value links among the test products and across the Synopsys Galaxy Design Platform to enable faster turnaround time meeting both design and test goals, higher defect coverage and faster yield ramp.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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