Synopsys Enables Superior Verification Planning and Coverage Analysis with Verdi Coverage

MOUNTAIN VIEW, Calif., Oct. 14, 2014 /PRNewswire/ -- **Highlights:**

- Verdi, the industry's open debug platform, now provides innovative planning and coverage technology integrated across all debug views, which allows users to quickly analyze and cross-probe holes identified through coverage analysis
- Provides the ability to quickly generate verification plans and link them to specification and requirements documents to ensure that projects stay on track as high-level requirements change
- Integrated with regression management solution, enabling users to execute verification tasks, view results and triage data to meet coverage goals and achieve verification closure more quickly
- Supports integrated visualization of results across simulation static checking, formal verification, verification IP (VIP) and FPGA-based prototyping solutions to deliver a unified view of verification closure

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of its Verdi® Coverage advanced planning and coverage technology. This solution addresses the growing challenge of verification closure for complex system-on-chips (SoCs) by introducing advanced technology that allows users to quickly create efficient verification plans, integrate third-party and user-defined metrics, link plans to requirement documents, and intuitively track project and test-level metrics across simulation, static checking, formal verification, VIP and FPGA-based prototyping. Verdi Coverage enables users to understand project progress, manage regression data, launch verification jobs, track project trends, generate reports and ultimately optimize resource allocation.

"As a leading design and verification services company, we work with leading-edge SoC companies to successfully shorten time-to-revenue and minimize schedule risks which require extensive upfront verification planning, flexible regression management and sophisticated coverage analysis," said Ambar Sarkar, chief verification technologist at Paradigm Works. "With its integrated coverage and debug capabilities, Verdi Coverage enables our teams to collaborate, identify the root cause of coverage holes and quickly drive clients' projects to verification closure."

Synopsys' innovative planning and coverage analysis technology is built on top of the Verdi environment recognized for being optimized, extensible and easy to use. Fully integrated with all Verdi debug views, it allows users to quickly analyze and cross-probe any holes identified through coverage analysis. It is also interoperable across a wide range of solutions including simulation, static checking, formal verification, VIP and FPGA-based prototyping. This unique level of integration and interoperability provides a unified view of project status that allows users to focus only on tasks required to improve the predictability of verification closure.

"We have been collaborating closely with many SoC leaders on advanced planning and coverage technology, which is essential to effectively address the verification closure challenges of complex SoCs," said Yu-Chin Hsu, vice president of R&D in the Synopsys Verification Group. "We have made a significant investment in verification planning and coverage visualization to address these challenges. Verification planning, coverage analysis and debug are fundamental elements of the Verification Compiler™ product, providing our customers with superior technology to help them meet their ever-shrinking schedules."

Availability

Verdi Coverage is available in limited customer availability (LCA) today. The advanced planning and coverage technology is also included as part of Synopsys' Verification Compiler product, also currently in LCA. Both products are planned for general availability in December 2014.

A technical webinar on Verdi Coverage, titled "Reinventing Coverage and Planning with Verdi—A Fully Integrated, Complete Verification Closure Flow To Help You Deliver Chips On Time," is now available for viewing.

About Synopsys

Synopsys, Inc. (NASDAQ:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934 regarding the expected release and benefits of the Verification Compiler product and the Verdi product. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900, ext.115
lgmartin@mcapr.com

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