# New DesignWare ARC HS38 Processor Doubles Performance for Embedded Linux Applications

Successor to Popular ARC 770D Core Delivers Significant Performance Increase, Support for 40-bit Physical Addresses and L2 Cache

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**Highlights:**

- New 32-bit ARC HS38 processor core is based on the extensible ARCv2 architecture and is optimized for growing number of embedded applications running Linux
- Delivers more than 4200 DMIPS in typical 28-nm processes while consuming less than 90 milliwatts of power and only 0.21 $mm^2$ of silicon area
- Optimized for high-end networking, automotive and digital home applications running embedded Linux
- Single-, dual- and quad-core configurations with support for Level 1 cache coherency, Level 2 cache and symmetric multiprocessing (SMP) offer scalable performance
- Robust ecosystem of software development tools, hardware, middleware and operating systems, including an optimized Linux kernel, accelerate design of HS38-based systems

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced availability of the DesignWare® ARC® HS38 Processor, the latest addition to the ARC HS Family of high-speed processor IP cores. Like the previously-released HS34 and HS36 processors, the 32-bit ARC HS38 is optimized for power efficiency (DMIPS/mW) and area efficiency (DMIPS/$mm^2$) with additional features to support embedded Linux and other high-end operating systems. A single HS38 processor delivers up to 4200 DMIPS at speeds up to 2.2 GHz in typical 28-nanometer (nm) silicon, more than twice the performance of previous generation ARC 770D cores supporting Linux. The ARC HS38's performance and low power consumption make it ideally suited to address the growing embedded control and signal processing demands of devices such as home routers and gateways, data centers, digital TVs, networked appliances and automotive infotainment.

"We selected the ARC 770D for our NPS-400 network processor because of its unique combination of high performance and low power, along with its extensible instruction set," said Guy Koren, CTO at EZchip Technologies.  "The new ARC HS38 provides an exciting upgrade path, delivering much higher performance with the same number of processors, and improved overall channel density. A critical component of the NPS-400 project was support for SMP Linux to ease our customers' software programming. Our collaboration with Synopsys resulted in an optimized SMP Linux kernel, which will benefit ARC HS38 users as well."

The ARC HS Processor Family utilizes the next-generation ARCv2 instruction-set architecture (ISA), which enables the implementation of high-performance embedded designs with low power consumption and a small silicon footprint. The new HS38 processor has been optimized for embedded applications running Linux and offers excellent performance efficiency, delivering up to 1.93 DMIPS/MHz. On typical 28-nm processes, the HS38 achieves 2.2 GHz while consuming less than 90 milliwatts of power and occupying only 0.21 $mm^2$ of silicon area. The HS38 has a full-featured memory management unit (MMU) supporting a 40-bit physical address space and page sizes up to 16 megabytes (MBs), giving designers the ability to directly address a terabyte of memory with faster data access and higher system performance. The HS38 is also available in multicore configurations (dual-core and quad-core) with support for SMP Linux, full Level 1 (L1) cache coherency and up to 8 MBs of Level 2 (L2) cache. In addition, an optional floating-point unit (FPU) accelerates computations with support for single- and double-precision arithmetic instructions. As with all ARC processors, the ARC HS38 is highly configurable, so users can determine the optimum hardware features to implement for their specific design, as well as extensible to enable the creation of user-defined hardware accelerators that are tightly coupled to the processor core.

"Synopsys has developed a compelling successor to it its popular ARC 770D Processor with the new ARC HS38," said Linley Gwennap, principal analyst of The Linley Group. "The systems deployed in home routers, mobile internet and auto infotainment applications are becoming increasingly complex, demanding greater functionality and performance without increasing energy consumption. With its 40-bit physical address space, L1 cache coherency and L2 cache support, the ARC HS38 processor is uniquely positioned to address the needs of these rapidly evolving high-end embedded applications, now and in the future."

The new HS38 Processor is supported by the Synopsys MetaWare Development Toolkit, a complete solution for developing, debugging and optimizing embedded software on ARC processors. The kit includes an optimized C/C++ compiler to generate highly efficient code, a debugger for maximum visibility into the software and a

fast instruction set simulator (ISS) for pre-hardware software development. An ARC HS Processor Family Virtualizer™ Development Kit (VDK) consisting of a processor and common peripherals is also available to run and debug software on a virtual prototype ahead of SoC availability. A fully cycle-accurate simulator is available for design optimization and verification. Open source software support for the HS38 Processor includes an optimized Linux kernel as well as the GNU Compiler Collection (GCC), GNU Project Debugger (GDB) and associated GNU programming utilities (binutils). For software development on hardware, the ARC AXS103 Software Development Platform provides a complete development environment with a rich set of peripherals, drivers, pre-built Linux images and application examples. Additional hardware and software tools supporting software development for ARC HS processors are available from third-party partners, giving developers the flexibility to choose the best and most familiar tools for their design project.

The ARC HS Processor Family offers designers unique features that ease system-on-chip (SoC) integration and improve system-level performance. Support for close coupled memories and direct mapped peripherals with single cycle access to all peripheral registers on an SoC improves performance and reduces system latency. The ARC Processor EXtension (APEX) technology enables user-defined hardware to be added to the core through custom instructions or user-supplied RTL, accelerating application-specific code while reducing power. The HS cores, including the new HS38, are also highly configurable so they can be customized for each instance on an SoC. Support for I/O coherency, native ARM® AMBA® AXI™ and AHB™ standard interfaces that are configurable for 32-bit or 64-bit transactions and an optional FPU that supports both single- and double-precision operations enable the HS processors to be implemented with the optimal combination of performance and energy consumption.

"With each new generation of electronic devices, SoC developers must satisfy the demand for additional performance and features with shrinking form factors and power budgets," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "Increasingly, we see Linux being used in high-end embedded applications. The HS38 enhances Synopsys' existing portfolio of ARC processors supporting high-level operating systems, bringing the high-performance capabilities of the ARCv2 architecture and HS family to designers of Linux-based embedded systems."

**Availability & Resources**
The DesignWare ARC HS38 Processor, ARC HS Family VDK and ARC AXS103 Software Development Platform are planned for general availability in December, 2014. An ARC HS38 technology plug-in for Synopsys' Lynx Design System, also available in December 2014, provides pre-tuned design flow scripts, constraints and tool settings for accelerating chip-level integration and time to optimized results. The MetaWare Development Toolkit, Linux kernel and GNU Toolchain are available now.

For more information, visit: http://www.synopsys.com/arc.

**About DesignWare IP**
Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controller, PHY and next-generation verification IP, analog IP, embedded memories, logic libraries, processor solutions and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and customized IP subsystems for rapid integration of IP into SoCs. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

**About Synopsys**
Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

**Forward Looking Statements**

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934 regarding the expected release and benefits of the DesignWare ARC HS38 Processor. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from

those anticipated in these forward-looking statements, even if new information becomes available in the future.

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