HiSilicon Chooses Synopsys' PrimeTime ADV for Faster Timing Closure

Achieves Single-pass Timing and Power ECO Closure on Multiple Tapeouts Including FinFET

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Highlights

- HiSilicon has chosen PrimeTime ADV for timing closure in advanced IC design flow
- Accurate single-pass timing and power closure with outstanding quality of results (QoR)accelerate time to market
- HiSilicon achieves multiple successful tapeouts with PrimeTime ADV, including their first FinFET design

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that HiSilicon Technologies, a leading end-to-end chipset solution provider for telecom network, wireless terminal and digital media, has chosen Synopsys' PrimeTime® ADV product for timing closure. The latest technology innovations in PrimeTime ADV, including signoff-driven, physically-aware engineering change order (ECO) and power recovery, were essential to accelerating design closure on key HiSilicon projects.

"At HiSilicon, time-to-market is a critical factor of our success in the competitive communications market," said Bruce Bin, sr. director, HiSilicon Technologies Co., Ltd. "Deploying a design flow that delivers fast, high-quality results can accelerate our design cycle by valuable weeks. As a result, we have chosen PrimeTime ADV for our design closure flow for all projects at various technology nodes. On a recent 16-nm FinFET tapeout, PrimeTime ADV provided fast, accurate and predictable design closure that helped us reach aggressive performance and power targets on time."

HiSilicon has deployed new PrimeTime technologies to ensure signoff-accurate and rapid design closure with Synopsys' Galaxy™ Design Platform, including:

- Advanced waveform propagation for signoff-accurate results on FinFET designs, including impact of increased Miller effect and resistance
- Placement density-aware ECO to achieve a 99.7 percent single-pass fix rate and excellent convergence with IC Compiler™ minimal physical impact (MPI) technology, resulting in 0.1 micrometer average cell movement
- Route-based ECO insertion to provide best QoR and minimize route change during IC Compiler ECO implementation
- Leakage recovery to reduce leakage power up to 10 percent in addition to IC Compiler final-stage leakage recovery with no signoff timing impact

"HiSilicon is one of the leading chipset solution providers in the competitive wireless and networking markets, where timing closure is a key focus," said Antun Domic, senior vice president and general manager, Synopsys Design Group. "Our partnership with HiSilicon has benefitted both companies by creating unique technologies in PrimeTime ADV, and we are pleased that they have chosen it for their design closure flow."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

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