Synopsys Releases Verification IP for Mobile PCIe Technology

Native SystemVerilog-based VIP for PCI Express architecture now supports M-PCIe technology, with built-in coverage, verification plan and protocol-aware debug

MOUNTAIN VIEW, Calif., Oct. 7, 2014 /PRNewswire/ -- Synopsys, Inc. (NASDAQ: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of verification IP (VIP) for the M-PCIe™ protocol, including built-in M-PHY® as defined by the MIPI® Alliance specification. Based on its native SystemVerilog VIP architecture, Synopsys' VIP for M-PCIe technology enables enhanced performance, ease of use and debug in SystemVerilog UVM environments. The Synopsys VIP for M-PCIe is integrated with Synopsys' Verdi® Protocol Analyzer, a protocol-aware environment that speeds debug by providing simplified views of protocol traffic. The addition of M-PCIe technology to Synopsys' VIP for PCI Express® architecture provides mobile and low power PCI Express design and integration teams with a full-featured, SystemVerilog UVM solution to accelerate verification and coverage closure.

"As an active PCI-SIG member, Synopsys has been a valued contributor to the advancement of PCIe technology," said Al Yanes, PCI-SIG chairman and president. "The Synopsys VIP support for the M-PCIe architecture further helps the PCI Express ecosystem attain adoption within an increasing range of platforms."

"The release of new protocol versions to address new market segments creates a complex and lengthy ramp-up process for design teams as they strive to rapidly verify compliance against the new specification," said Debashis Chowdhury, vice president of R&D for the Synopsys Verification Group. "We continue to deliver VIP for new versions of protocols to enable our customers to achieve their SoC verification closure goals and accelerate time-to-market. The new Synopsys' VIP for M-PCIe protocol provides designers with the built-in protocol knowledge, features and methodology support to save time, increase design quality and meet project schedules."

The VIP for M-PCIe is a part of Synopsys' comprehensive verification IP portfolio for PCIe, which supports all versions of the PCIe technology and NVMe. Synopsys' complete M-PCIe IP solution consisting of verification IP, a silicon-proven DesignWare® M-PCIe digital controller and M-PHY enables project teams to accelerate development of M-PCIe-based SoCs and hit critical market windows.

Synopsys will be demonstrating verification IP support for M-PCIe at the MIPI Alliance All Members Meeting in Shanghai October 6-10: https://www.synopsys.com/IP/Pages/mipi-f2f-shanghai-event.aspx

Availability

Synopsys' verification IP for M-PCIe is available today for early adopters as a stand-alone title and as part of Synopsys' Verification IP Library as well as Verification Compiler™. The DesignWare M-PCIe digital controller and PHY are available now. www.synopsys.com/vip.

About Synopsys Verification IP

Synopsys VIP, based on its next-generation architecture and implemented in native SystemVerilog, offers native performance, native debug with Verdi Protocol Analyzer, enhanced VIP ease of use, configurability, coverage and source code compliance test suites. These capabilities substantially increase user productivity for one of the most difficult and time-consuming aspects of SoC design and verification. Synopsys VIP library includes a broad portfolio of interface, bus, and memory protocols.

About Synopsys

Synopsys, Inc. (NASDAQ:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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