TSMC and Synopsys Accelerate Custom Design Productivity for 16FF+ Process

Collaboration Enables Best Practices for Custom Implementation Productivity with FinFET Devices

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Highlights:

- Synopsys custom design solution enhanced to meet emerging requirements for 16FF+ process
- Schematic and simulation environment enhanced to simplify parasitic-aware circuit simulation
- Layout solution enhanced for matching device placement, guard ring creation and dummy insertion features to speed creation of analog layout with FinFET devices

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that it has collaborated with TSMC to develop an expanded 16FF+ custom design reference flow using Synopsys' custom design solution. Part of TSMC's design infrastructure, the expanded custom reference flow adds new technologies to the schematic and layout environment to streamline and accelerate custom design for TSMC's 16FF+ process. Highlights of these improvements include new methods for design constraints management, estimation of layout-dependent effects prior to final layout, schematic-driven layout with FinFET devices, a simplified method to run pre- and post-layout simulation, and a streamlined graphical user interface for layout of matched devices and guard rings.

"Our customers need EDA tools, a design methodology and IP to all be in place when they are ready to adopt a new process technology," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division. "We worked closely with Synopsys to ensure that complete custom design solutions for the 16FF+ process node are available to our customers."

Enhancements to the Galaxy Custom Designer® Schematic Editor and Simulation Environment
In 16FF+ design, circuit designers need a smooth path for communicating constraints to the layout designer, and Synopsys provides a comprehensive solution for constraint management. Design constraints such as device matching, color assignment, symmetry and clustering can be added to schematics and passed to the layout editor to be enforced during layout. Additionally, the schematic environment has been updated with a simplified method for running pre- and post-layout circuit simulation and comparing the results. Speeding the analysis of layout parasitics reduces the time it takes to finalize the layout. The schematic environment has also been enhanced to support a schematic-driven layout flow for FinFET devices.

Enhancements to the Laker® Layout Editor
In analog circuits, good device matching is needed to deliver performance margin and production yield. The matching device creator in Laker makes it easier to achieve quality custom layout with updated support for matched placement of FinFET devices. Now, density-aware device array placement, guard ring creation and dummy insertion are all handled through a simple graphical user interface (GUI). For analyzing layout-dependent effects, the custom design reference flow with Laker and TSMC's LDE-API provides a smooth path for back-annotating extracted device parameters to simulation after placement is completed.

"We have had a multi-year collaboration effort with TSMC in custom design which spans 3D extraction, SPICE modeling, physical verification and improved custom layout productivity. This latest collaboration with TSMC delivers best practices and technologies for custom implementation with FinFET technology," said Bijan Kiani, vice president of product marketing at Synopsys. "Customers who have adopted this solution are seeing significant productivity gains while benefiting from the advantages of 16FF+ process technology."

About Synopsys
Synopsys, Inc. (Nasdaq: SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at https://www.synopsys.com.

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