# Synopsys Tools Achieve TSMC Certification for 16-nm FinFET+ Process and Both Companies Enter 10-nm FinFET Collaboration

Certification of Digital and Custom Tools Enables Early Adopters to Realize QoR Benefits of the New Processes

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**Highlights:**

- Digital and custom tools from Galaxy™ Design Platform are ready for TSMC 10-nm FinFET and 16-nm FinFET+ processes
- Successful 10-nm digital design flow pipe-cleaning using the Galaxy Design Platform on ARM® Cortex®-A15 MPCore™ processor
- TSMC 16-nm FinFET+ Reference Flow delivered

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that TSMC has certified a comprehensive list of Synopsys' custom and digital design tools for their 16-nm FinFET+ processes. The V0.9 certifications are all completed and V1.0 certification is on-track and to be concluded by November, 2014. The two companies have also entered N10 collaboration. With needed tool enhancements in place to meet 10-nm FinFET process requirements, customers can now use Synopsys tools for their 10-nm design starts.

Collaboration between TSMC and Synopsys is enabling customers to deploy Synopsys' industry-leading digital and custom tools to take advantage of the power, performance and area benefits of the 10-nm and 16-nm process technologies. The extensive engineering collaboration between Synopsys and TSMC facilitated delivery of key technologies including routing rules, physical verification runsets, extraction technology files, interoperable process design kits (iPDKs) and a reference flow for the N16FF+ process. System-on-Chip (SoC) design teams can now deploy the silicon-proven, project-ready Synopsys solution to implement FinFET-based designs.

"Our deep and extensive collaboration with Synopsys on critical design-enablement technologies has continued beyond the N16FF process," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division at TSMC. "Jointly, Synopsys and TSMC are addressing our customers' needs to deliver highly optimized design solutions for N10FF and N16FF+ process geometries."

"Our goal is to enable our mutual customers to maximize the power, performance and area benefits of the 10nm and 16-nm FinFET process technologies," said Bijan Kiani, vice president of product marketing, Design Group, at Synopsys. "This extensive technology collaboration spans the digital and custom tools to allow engineers to deliver their next-generation designs in a productive and predictable manner."

Key Synopsys tools enabled by the TSMC and Synopsys collaboration for 10 nm include:

- The IC Compiler™ product:  The key product for early process enablement and rule formulation delivers support for routing and placement enablement, color-aware timing closure and signal electromigration (EM)
- IC Validator: Design rule checks (DRC), layout vs. schematics (LVS) and metal fill
- The StarRC™ solution: Multi-patterning support, color-aware variation modeling and 3-D FinFET silicon profile modeling using the QuickCap® field solver
- The PrimeTime® solution: Signoff accurate delay calculation and timing analysis with advanced waveform propagation includes impact of ultra-low voltage, increased Miller Effect and resistivity
- PrimeRail: Accurate static and dynamic IR-drop analysis, and power/ground (P/G) EM rules support
- NanoTime: Static timing analysis of embedded SRAMs
- Galaxy Custom Designer® schematics: Display mask color on schematic, assign color constraints and check schematics for color conflicts
- The Laker® Layout tool: Support for 10-nm full coloring flow; reads color constraints from Galaxy Custom Designer schematic and enforces during layout; design-rule-driven color checking during layout and IC Validator integration to support color-aware verification and color back annotation
- The HSPICE®, CustomSim™ and FineSim® simulation products: Support 10nm FinFET device modeling with self-heating effect and deliver accurate circuit simulation results for the latest FinFET-based designs
- CustomSim-RA: Support for 10-nm electro-migration (EM) rules for accurate transistor level EM and IR-drop analysis

**About Synopsys**

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

**Forward-looking Statements**

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934 regarding the expected V1.0 certification by TSMC. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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