Synopsys Unveils Verification Continuum to Enable Next Wave of Industry Innovation in Software Bring-Up for Complex SoCs

Next-Generation Verification Platform to Accelerate Time-to-Market by Months

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Highlights:

- Increasing System-on-Chip (SoC) complexity and software content combined with rising time-to-market pressures are driving the need for a next-generation verification solution that spans pre-silicon verification, post-silicon validation and early software bring-up.
- SoC verification requires multiple engines, and migrating designs between engines can take months. Synopsys' Verification Continuum™ platform, developed in collaboration with market leaders, unites Synopsys' best-in-class verification solutions, facilitating a seamless transition between them and improving SoC time-to-market by months.
- Verification Continuum is built from the industry's fastest engines developed by Synopsys – Virtualizer™ virtual prototyping, Verification Compiler™ static and formal technologies, VCS® simulation, ZeBu® emulation, HAPS® FPGA-based prototyping and Verdi® debug.
- Verification Continuum introduces Unified Compile with VCS to provide seamless transitions between verification engines and up to 3X faster emulation compile time, and Unified Debug with Verdi to provide debug continuity across all domains and abstraction levels to enable dramatic increases in debug efficiency.
- Verification Continuum is architected with FPGA-based emulation and prototyping, delivering the speed and scalability required for software bring-up and SoC verification.

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the Synopsys Verification Continuum platform to accelerate industry innovation for earlier software bring-up and shorter time-to-market for advanced SoCs. Verification Continuum is built from Synopsys' market-leading and fastest verification technologies providing virtual prototyping, static and formal verification, simulation, emulation, FPGA-based prototyping and debug in a unified environment with verification IP, planning and coverage technology. Verification Continuum introduces Unified Compile with VCS and Unified Debug with Verdi across the verification flow, speeding time-to-market by months for complex SoC designs.

"AMD's advanced multi-core Accelerated Processor Unit designs require a continuum of verification technologies working seamlessly together to meet growing hardware and software verification requirements," said Alex Starr, fellow & pre-silicon solutions architect at AMD. "Synopsys Verification Continuum represents an important new direction for the industry, and our initial evaluation of the technology indicates it can accelerate design schedules with a more efficient and scalable platform optimized for complex SoC verification and early software bring-up."

The mobile and Internet of Things (IoT) markets are driving dramatic increases in SoC complexity and software content along with intensifying time-to-market pressure. To address these challenges, SoC teams require many verification technologies such as simulation, emulation and prototyping across the spectrum of pre-silicon verification, post-silicon validation and early software bring-up. Today engineers spend months of effort in design bring-up and transition effort between disjoint technologies, further complicated by the need to debug across domains and to support large software teams. To shorten SoC time-to-market, leading teams are adopting "shift-left" strategies with concurrent practices across pre-silicon verification, post-silicon validation and software bring-up. Synopsys' Verification Continuum enables these shift-left strategies with best-in-class verification technologies unified with seamless design bring-up, transition and debug throughout the flow.

Industry's Fastest Verification Engines

Synopsys' Verification Continuum is built from the industry's fastest verification engines including Virtualizer virtual prototyping, Verification Compiler static and formal technologies, VCS simulation, ZeBu emulation, HAPS FPGA-based prototyping and Verdi^{3}™ debug. These best-in-class technologies provide the performance and capacity that industry leaders depend on to verify many of the world's largest and most complex chips.

Unified Compile with Industry-Leading VCS

Verification Continuum features Unified Compile based on the mature VCS simulator front-end, providing a robust simulation-like user experience across the verification flow, that enables engineers to easily transition between simulation, static and formal verification, emulation, FPGA-based prototyping and debug as required by the verification task. Existing flows based on individual point tools require extensive setup for each tool in the flow, and weeks or months of effort to move a design between

different tools based on varying language support or other requirements. Unified Compile with VCS eliminates this redundant work, saving months of effort in typical project schedules.

Unified Debug with Verdi

Unified Debug based on Synopsys' Verdi^3 environment provides a consistent debug user experience across the verification flow, optimized with Verification Continuum technologies for even higher productivity. Verdi^3 has long been recognized as the leading open debug platform, and as part of the Verification Continuum, it provides a single interface for multi-domain debug across virtual prototyping, static and formal verification, simulation, emulation and FPGA-based prototyping. Since bugs may exist on the boundary between traditional verification domains, Verdi^3 also enables fully synchronized, mixed-abstraction debug between SPICE, RTL, transactions and software.

Scalable FPGA-Based Emulation and Prototyping

As SoC complexity and software content increase, leading SoC development teams have concluded that commercial FPGA-based hardware-assisted verification is the best, most scalable approach to meet the growing demand for high-performance platforms for early software bring-up and SoC verification. Verification Continuum integrates FPGA-based emulation and prototyping seamlessly into mainstream verification flows, helping to save weeks to months in design bring-up time compared with earlier approaches. Verification Continuum's Unified Compile technology has been architected to support FPGA-based verification platforms, delivering up to 3X faster compile time for Synopsys' ZeBu Server-3 emulation system.

"The Verification Continuum requires an optimized software flow combined with the highest-performance, highest-capacity emulation and prototyping hardware," said Victor Peng, executive vice president and general manager of the Programmable Products Group at Xilinx. "Xilinx has raised the bar again with our Virtex® UltraScale™ devices, offering the largest 20nm FPGA in the industry, the XCVU440. We are working closely with Synopsys to optimize our Vivado® Design Suite flow to address the unique requirements of hardware-assisted verification users."

"Synopsys' Verification Continuum, developed in close collaboration with market leaders, will enable a new era of SoC verification for the industry," said Manoj Gandhi, senior vice president and general manager of the Verification Group at Synopsys. "The significant verification R&D investments Synopsys has made over the past two years are already showing promising early results towards helping customers reduce time-to-market by months for advanced SoC designs."

Availability

Early availability is scheduled for December 2014, with general availability in 2015.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934 regarding the expected release and benefits of the Verification Continuum platform. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900, ext. 115

lgmartin@mcapr.com

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