Users Cite 10 Percent Smaller Design Sizes with Latest Releases of Synopsys' Design Compiler

New Innovations Also Reduce Leakage Power and Accelerate Design Schedules

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Highlights:

- Elmos Semiconductor reports up to 10 percent reduction in gate count on mixed-signal design
- KYOCERA Document Solutions reports 10 percent smaller area
- New monotonic area optimization engine provides improvements in area and power while preserving timing results

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that multiple customers have achieved smaller area using the latest releases of its Design Compiler® RTL synthesis solution, a key component of Synopsys' Galaxy™ Design Platform. Aggressive area optimization is critical for designers across a wide range of electronic applications to either lower system costs or implement additional functionality without increasing die size. Innovations in the latest releases include advanced optimizations operating with and without physical information, which lower power and produce smaller, more routable designs without impacting timing.

"Minimizing area and meeting timing requirements enables us to differentiate and deliver value in a highly competitive multi-functional product marketplace," said Michihiro Okada, general manager of the Software 3 R&D Division, Corporate Software Development Division at KYOCERA Document Solutions Inc., a leading manufacturer of document imaging solutions and document managing systems. "Design Compiler's new monotonic area optimization reduced design area by 10 percent for multiple designs while meeting timing requirements and lowering leakage power. This allowed my design team to implement additional functionality without an increase in die cost."

"As a leader in mixed-signal semiconductors for the automotive, industrial and consumer markets, reducing die size is critical to meeting our business objectives," said Armin Kemna, director Design Support at Elmos Semiconductor. "We are seeing up to 10 percent reduction in gate count simply by using the latest release of Design Compiler. In addition, technology links between Design Compiler and IC Compiler provided early insight into physical challenges and helped us stay on schedule."

Design Compiler includes new optimization technologies that monotonically reduce design area and leakage power by an average of 10 percent while maintaining timing quality of results (QoR). These area optimizations operate on new or legacy design netlists, with or without physical information and at all process nodes. Utilizing this new capability, in conjunction with new congestion optimizations, designers can significantly reduce die area and ease design closure without impacting any other QoR metrics. In addition, new RTL analyses and cross probing capabilities accelerate design schedules.

"Smaller die size and shorter design schedules continue to be key requirements for our customers designing at both established and emerging process nodes," said Bijan Kiani, vice president of marketing for Synopsys' Design Group. "These new technologies for smaller area and lower power consumption help our customers to be more competitive in their market segments, while strengthening Design Compiler's position as the synthesis tool of choice for designers worldwide."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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