Synopsys' New DesignWare MIPI D-PHY Cuts Area and Power by 50 Percent

Industry-First Support for MIPI D-PHY v1.2 Specification Increases Performance to 2.5 Gbps While Lowering Cost for Image Sensor and Display Applications

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Highlights:

- DesignWare MIPI D-PHY is 50 percent lower in area and power compared to competitive solutions, reducing silicon cost and extending battery life
- Compliance to the MIPI D-PHY v1.2 specification delivers aggregated data throughput of up to 20 Gbps for high-resolution imaging applications
- Proven interoperability with Synopsys DesignWare MIPI CSI-2 and MIPI DSI Controllers combined with MIPI verification IP provides a complete, verified solution that reduces integration risk
- Configurability options enable targeting multiple applications with the same SoC

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that it has cut the area and power consumption of its DesignWare® MIPI® D-PHY™ by 50 percent compared to competitive solutions while increasing performance to 2.5 Gbps per lane, reducing system-on-chip (SoC) silicon cost and extending battery life for mobile, consumer and automotive applications. Compliant to the MIPI D-PHY v1.2 specification and part of a complete solution with DesignWare MIPI DSI and CSI-2 Controllers and verification IP (VIP), the D-PHY reduces integration risk and the effort of connecting to a variety of image sensors and displays.

"The DesignWare MIPI D-PHY offered low power consumption, high performance and configurability options that were critical to the success of our Myriad 2 Vision Processing Unit," said Sean Mitchell, senior vice president and COO at Movidius. "Using Synopsys' high-quality MIPI IP solutions that support the latest specifications and features helps us quickly incorporate needed functionality into our SoCs with less risk."

"Over the last 10 years, Synopsys has played an active role in MIPI Alliance working groups, contributing to the development and proliferation of MIPI Alliance technology," said Joel Huloux, chairman of the board of MIPI Alliance. "With the introduction of the latest DesignWare MIPI D-PHY, Synopsys helps designers take advantage of the high-performance and low-power capabilities specified in the D-PHY v1.2 specification to quickly deploy SoCs for high-end mobile, consumer and automotive image sensor and display applications."

"To accelerate their time-to-market, designers of high-resolution products require proven IP that helps lower the risk of incorporating the interfaces into their SoCs," said Jurgen Beck, vice president and general manager at Keysight Technologies. "Our measurement tools and Synopsys' new D-PHY IP help support and develop the entire MIPI ecosystem, and we look forward to collaborating with Synopsys on future MIPI developments."

The DesignWare MIPI D-PHY is the physical layer used for MIPI CSI-2 and DSI Host and Device applications to connect image sensors and displays to SoCs in mobile and embedded applications. The DesignWare MIPI D-PHY is the first D-PHY that is compliant to the MIPI Alliance D-PHY v1.2 specification, enabling operation speeds up to 2.5 Gbps per lane. For high-resolution output, four lanes of the DesignWare MIPI D-PHY can be aggregated to support 10 Gbps speeds and eight data lanes can be aggregated to achieve 20 Gbps speeds. In addition, the DesignWare MIPI D-PHY's configurability options enable designers to reduce the number of SoC designs required to target multiple applications, minimizing time-to-market.

"By delivering an extremely small-area and low-power D-PHY to the fast-paced and competitive mobile market, Synopsys helps designers differentiate their SoCs in both silicon cost and battery life," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "With a broad portfolio of high-quality IP supporting the latest MIPI Alliance standards, Synopsys enables designers to integrate the latest functionality into SoCs for the mobile and consumer markets."

Availability
The new DesignWare MIPI D-PHY is available now in 16-nm FinFET processes, with availability in 28-nm processes scheduled for early 2015. VIP for MIPI D-PHY v1.2 is available now.

About DesignWare IP
Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controller, PHY and next-generation verification IP, analog IP, embedded

memories, logic libraries, processor solutions and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and customized IP subsystems for rapid integration of IP into SoCs. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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