Cavium Standardizes on Synopsys' IC Compiler for High-performance Processor-based SoC Designs

Latest Release Delivers Higher Performance and Lower Power for Advanced Design

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Highlights:

- Highest operating frequency achieved through pre-route look-ahead technologies
- Concurrent dynamic and leakage power optimization targets FinFET-based process technology
- Faster design closure using PrimeTime physically-aware ECO

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of the 2014.09 release of its IC Compiler™ place and route product, a key component of Synopsys' Galaxy™ Design Platform. The latest release continues the well-established trend of enabling leading-edge system on a chip (SoC) design through improved quality of results, faster convergence and advanced support for FinFET-based design. New capabilities include look-ahead technologies and enhanced concurrent clock and data optimization (CCD) for a frequency boost on high-performance designs, accelerated design closure using Synopsys' PrimeTime® physically-aware engineering change order (ECO) and cutting-edge optimizations to reduce power and improve timing for FinFET-based emerging silicon technologies.

"Cavium is a market leader in high-performance processors used to power a wide array of networking applications around the world," said Anil Jain, corporate vice president, IC engineering at Cavium. "We have long relied on IC Compiler to provide us with new, leading-edge technologies that enable us to achieve the best performance across all our complex and challenging designs. The latest release helps us further our leadership position in the marketplace."

The new release builds on a very important concept of look-ahead, which was introduced in the previous release of IC Compiler. A technique especially critical for high-performance designs, look-ahead tries to predict downstream processing at early stages of the design when all the information, such as detailed wiring, is not yet available. In 2013, look-ahead encompassed the use of actual route topologies to identify and avoid congestion, faster wires to boost timing and enhanced modeling to accurately predict downstream wire delays. The 2014.09 release delivers more look-ahead technologies including accounting for downstream effects such as crosstalk at the pre-route stage and performing virtual optimizations during placement for improved timing. CCD, a key technology to increase on-chip clock frequency, has been augmented to more accurately account for the timing impact of signal integrity and detailed wiring, yielding up to five percent faster circuits.

IC Compiler, working hand-in-hand with Synopsys' PrimeTime, provides a highly efficient physically-aware ECO solution to minimize the number of ECOs and implement them with minimal layout perturbation. It also has a consistency checker that automatically identifies and resolves differences between the signoff and place-and-route environments to improve signoff correlation. This new release provides expanded coverage of the consistency checker and multivoltage-aware on-route ECO implementation for faster design closure.

Beyond basic manufacturing compliance for FinFETs, the 2014.09 release addresses several second order effects that are critical to delivering quality results on FinFET-based designs. In this software release, dynamic power is optimized simultaneously with leakage power, timing, area and routability in order to achieve the maximum total power savings and meet timing. Additionally, the release addresses the pin accessibility challenge for small, highly optimized cells in order to retain the benefits of miniaturization.

Emerging process nodes are characterized by highly resistive wires which can lead to signal distortion that impacts layout-to-silicon correlation. Also, on-chip variation (OCV) effects are more severe and cannot be adequately addressed by margining. The previous release addressed these challenges through more accurate signal modeling to enable tighter silicon correlation and the introduction of parametric OCV (POCV), a lightweight statistical margining approach to generate higher performance circuits. The 2014.09 release furthers POCV accuracy and incorporates advanced optimizations to reduce wire resistance.

"As a leading provider of high-performance SoCs, Cavium has been an early adopter of each emerging process node while pushing the envelope on performance and power," said Antun Domic, executive vice president and general manager, Design Group at Synopsys. "Our close collaboration has helped drive many state-of-the-art technologies in IC Compiler and led to its widespread deployment as the standard place-and-route tool across all of Cavium."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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