Wipro Accelerates SoC Verification with Synopsys Verification IP Portfolio

Native SystemVerilog-based VIP Used in Advanced Testbench Methodology Environment to Address SoC Verification Challenges

MOUNTAIN VIEW, Calif., Sept. 10, 2014 /PRNewswire/ -- Synopsys, Inc. (NASDAQ: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that Wipro Ltd. has adopted Synopsys' broad portfolio of native SystemVerilog UVM-based verification IP (VIP) for on-chip buses, interfaces and memories used on systems-on-chips (SoC) designs. Wipro will use this broad portfolio with its UVM testbench environments to reduce verification time, increase quality and accelerate customer schedules. The availability of source code UVM compliance test suites further assists Wipro to rapidly achieve coverage goals and increase their confidence in the robustness of the SoC interfaces.

"Wipro provides premium verification services across the industry for a wide variety of SoC designs and prides itself on its high quality and on-time completion of projects. To achieve this, we utilize the most advanced methodologies and technologies," said Prasad Bhatt, vice president, Product Engineering Services, Wipro Ltd. "We have collaborated with Synopsys over many projects and depend on their high-quality verification IP and test suites, that fit our advanced UVM-based methodologies, to enable us to deliver high-quality and quick turnaround time to our customers."

Wipro has adopted Synopsys VIP for buses, interfaces and memory, including ARM® AMBA® interconnect, USB 3.0, MIPI CSI-2, MIPI DSI, PCI Express and SDIO. Synopsys' native SystemVerilog-based VIP includes built-in coverage, test plans, error injection, protocol-aware debug and test suites to accelerate time to verification closure. Native SystemVerilog-based VIP is easier to integrate and use in SystemVerilog UVM testbenches and removes the need for gaskets or wrappers that slow down performance.

"We have collaborated with many design verification teams to address the increasing challenges of SoC verification using advanced technologies. With the growing size and complexity of SoCs, VIP is becoming an increasingly important technology to verify chip designs," said Debashis Chowdhury, vice president of R&D for the Synopsys Verification Group. "With our portfolio of leading native SystemVerilog VIP for buses, interfaces and memories, we continue to offer SoC teams the verification and compliance environments needed to build and verify differentiated products and get them to market quickly."

About Synopsys Verification IP

Synopsys VIP is based on a next-generation architecture and implemented in 100 percent SystemVerilog, offering enhanced ease of use, configurability, performance, debug, coverage and extensibility. Synopsys' VIP supports Protocol Analyzer, a protocol-centric debug environment with visibility into the memory array for simplified debug. These capabilities substantially increase user productivity for one of the most difficult and time-consuming aspects of SoC design and verification. For more information, visit www.synopsys.com/vip.

About Synopsys

Synopsys, Inc. (NASDAQ:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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