Synopsys Showcases DesignWare IP Solutions for USB 3.1 and PCI Express 4.0 at Intel Developer Forum 2014

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, will showcase DesignWare® IP for USB 3.1 and PCI Express® 4.0 at the Intel Developer Forum (IDF) in San Francisco, California from September 9-11.

IDF is the premier global technology industry event bringing together technology professionals who are actively directing where technology is going. At IDF, attendees can experience visionary keynotes, technology and industry insights, and technical sessions. Synopsys will participate in the technology showcase that features exhibits and demonstrations from Intel and leading technology companies.

Featured DesignWare IP Demos

- SuperSpeed USB Community: Booth 773
  - USB 3.1 Technology Demonstration
  - USB 3.0 femtoPHY IP for 14-/16-nm FinFET Processes
  - USB 3.0 SSIC Host and Device IP Interoperating with MIPI M-PHY
- General Community: Booth 655
  - PCI Express 4.0 Controller IP
  - PCI Express PHY IP at 16 Gbps

For more information or to register now, please visit: http://www.intel.com/content/www/us/en/intel-developer-forum-idf/san-francisco/2014/idf-2014-san-francisco.html

WHAT: Intel Developer Forum

WHEN: September 9-11, 2014

WHERE: Moscone West, 747 Howard Street, San Francisco, CA, 94103

EXHIBIT HOURS: Sept 9: 11:00 am — 7:00 pm; Sept 10: 11:00 am —1:00 pm and 4:00 pm — 7:00 pm; Sept 11: 11:00 am — 2:00 pm

DEMO DESCRIPTIONS:

- **USB 3.1 IP Technology Demonstration**
  Synopsys will show 10 Gbps transfers over USB 3.1 using the Synopsys USB 3.1 Device and Host controller IP on Synopsys' HAPS® FPGA-based prototyping platforms.
- **DesignWare USB 3.0 femtoPHY IP on 14-/16-nm FinFET Processes**
  With up to 50% smaller die area and low power optimization, the DesignWare USB femtoPHY IP minimizes USB PHY silicon cost while extending battery life. The demonstration shows the femtoPHYs' margin in a 14-/16- FinFET process.
- **DesignWare USB 3.0 SSIC Host and Device IP with MIPI M-PHY**
  USB 3.0 SuperSpeed InterChip (SSIC) uses USB 3.0 protocols and the low power MIPI M-PHY for connecting WiFi and modem chips to mobile application processors to reduce power consumption by up to 67% in mobile devices. The demonstration shows theDesignWare USB 3.0 SSIC Host with MIPI M-PHY transferring data to a USB 3.0 Device with MIPI M-PHY on Synopsys' HAPS FPGA-based prototyping platform.
- **DesignWare PCI Express 4.0 Controller IP**
  Synopsys will demonstrate the industry's first PCI Express 4.0 Controller IP. The demonstration shows how to easily configure the DesignWare PCIe 4.0 IP for specific SoC requirements, including 16 Gbps data rates.
- **DesignWare PHY IP for PCI Express at 16 Gbps**
  Synopsys will demonstrate DesignWare PHY IP for PCI Express running at 16 Gbps. The 28-nm test chip includes four channels of high-speed 16 Gbps SerDes that are accessible through a Graphic User Interface for PHY configuration setup and performance monitoring.

For more information on DesignWare IP, please visit: https://www.synopsys.com/designware-ip.html

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com/.

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