Synopsys Cuts Area of DesignWare NVM IP for Automotive Grade 0 Applications by 75 Percent

New Trim NVM IP Leverages Faster Programming Times to Reduce NVM Test Time by 3X Without Compromising AEC-Q100 Quality

MOUNTAIN VIEW, Calif., July 8, 2014 /PRNewswire/ --

Highlights:

- Synopsys DesignWare® AEON® Trim Non-Volatile Memory (NVM) IP for high-voltage processes offers 75 percent smaller IP area compared to existing reprogrammable NVM IP solutions, reducing the cost and size of high-reliability automotive ICs
- Meets stringent automotive Grade 0 temperature (-40C to 150C) and AEC-Q100 quality requirements
- Faster programming times and specialized test modes reduce NVM test time by 3X compared to alternative IP offerings
- Reprogrammable NVM with 15+ year data retention helps ensure data stability in automotive and industrial safety systems

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of the DesignWare AEON Trim NVM IP for high-voltage processes. The new IP is up to 75 percent smaller than alternative NVM IP solutions, helping to reduce the size and cost of automotive ICs. Available in standard 180-nanometer (nm) 5V CMOS and Bipolar CMOS DMOS (BCD) processes without a need for additional masks or process steps, the DesignWare NVM IP supports the wide temperature range required for automotive Grade 0 applications and exceeds AEC-Q100 quality standards. In addition, faster programming times reduce NVM test times by 3X compared to alternative NVM solutions, enabling designers to reduce production test times and minimize test costs for automotive and industrial ICs.

"ZMDI's robust AEC-Q100-certified ICs provide advanced sensor-signal conditioning and configurability, and integrating the DesignWare AEON Trim NVM IP will help to ensure high data retention and reliability while minimizing area and test times," said Dr. Michael J. Ohletz, executive vice president, global and strategic quality at ZMDI. "Designers selecting components for demanding and harsh under-the-hood automotive environments look for proven IP solutions that can reliably perform crucial safety functions for 15 or more years. ZMDI selected Synopsys NVM IP because the IP met our rigid specifications and because of our shared commitment to producing reliable, high-quality products."

With the growth in the automotive IC market, designers need to meet the quality and reliability criteria established for the extreme environment under the hood of a car while respecting the cost and size parameters of even the smallest ICs. With its Grade 0 temperature range and 15+ year data retention capabilities, the DesignWare AEON Trim NVM IP for high-voltage processes enables designers to implement their ICs in applications with harsher and safety-critical environments.

The DesignWare AEON Trim NVM IP for high-voltage processes includes special test modes that increase programming speed and reduce test costs and time by up to 3X. For example, the IP includes bulk operations that enable designers to program the entire array in a single, faster operation. In addition, designers can select test conditions and test limits that emulate temperature effects, thereby eliminating the need for testing across temperature.

"Designers developing automotive ICs increasingly expect NVM IP providers to support the Grade 0 temperature range and AEC-Q100 standards while reducing IP area and cutting test times," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "Synopsys DesignWare AEON Trim NVM IP meets or exceeds their expectations in every area. More than 500 million ICs with DesignWare NVM IP ship each year. Synopsys' track record of delivering high-quality IP enables designers to meet the industry demand for smaller, cost-effective, high-performance ICs."

Availability

DesignWare AEON Trim NVM IP for high-voltage processes is available now in leading 180-nm 5V CMOS and BCD processes.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controller, PHY and next-

generation verification IP, analog IP, embedded memories, logic libraries, processor solutions and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and customized IP subsystems for rapid integration of IP into SoCs. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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