Synopsys Expands Verification IP Portfolio with Memory Models

DDR and LPDDR Verification IP Now Broadly Available

MOUNTAIN VIEW, Calif., June 3, 2014 /PRNewswire/ -- Synopsys, Inc. (NASDAQ:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the release of its DDR4/3 and LPDDR4/3/2 Verification IP (VIP) available as part of Synopsys' Verification Compiler™ solution and as standalone titles. Based on 100 percent native SystemVerilog, the memory VIP includes built-in support for RDIMM and LRDIMM models, Verdi® Protocol Analyzer debug capability and integrated verification plans, all designed to enable users to accelerate the verification of memory interfaces and achieve earlier system-on-chip (SoC) verification closure.

"To deliver the DDR3/DDR4 memory technologies in our advanced 64-bit AMD Opteron™ A-Series server SoC, formerly code-named 'Seattle,' we were an early user of the Synopsys DDR verification IP as part of a complete SystemVerilog UVM verification environment," said Charles Fielder, senior design manager at AMD. "Given the consistency with other Synopsys SystemVerilog VIP titles in use, we were able to rapidly and successfully deploy Synopsys' DDR VIP to successfully achieve our verification goals while meeting our aggressive schedule."

With debug being one of the most challenging elements of protocol verification, Verdi Protocol Analyzer provides protocol-centric debug, enabling users to quickly understand protocol activity, identify bottlenecks and quickly find and debug unexpected behavior. Furthermore, architected with native SystemVerilog and the UVM methodology, the Synopsys memory VIP titles do not require wrappers, translators, or remapping, and support all major simulators.

"Through our long-standing collaborations with SoC leaders we continue to expand our VIP offering as protocol verification is increasingly critical in SoC flows," said Manoj Gandhi, senior vice president and general manager of the Synopsys Verification Group. "We continue to invest in and innovate key VIP technology, including adding key memory titles to our portfolio, to address the escalating verification requirements and enable faster time-to-market for a wide range of SoCs."

Availability

Synopsys DDR4/3 and LPDDR3/2 memory VIP are available today. LPDDR4 is scheduled for early availability in Q3 2014. All memory VIP titles are included as part of the Synopsys VIP Library as well as Verification Compiler.

More information is available at www.synopsys.com/vip.

About Synopsys Verification IP

Synopsys VIP, based on its next-generation architecture and implemented in 100 percent SystemVerilog, offers enhanced VIP ease of use, configurability, performance, debug, coverage and extensibility. Synopsys' VIP supports Protocol Analyzer, a protocol-centric debug environment with visibility in the memory array for simplified debug. These capabilities substantially increase user productivity for one of the most difficult and time-consuming aspects of SoC design and verification. For more information, visit www.synopsys.com/vip.

About Synopsys

Synopsys, Inc. (NASDAQ:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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