Samsung and Synopsys Deliver Design Tools and IP for 14-nm FinFET Process

FinFET-ready Silicon-proven Tools and IP Available for Immediate Design of SoCs

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Highlights:

- Galaxy Design Platform certified for Samsung's 14-nm FinFET process, including Process Design Kit (PDK) for Samsung's foundry customers
- Silicon-proven DesignWare IP available now for Samsung's 14-nm FinFET process
- Design and IP solution deployed on 14-nm FinFET SoC product designs

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced certification and immediate availability of a comprehensive design solution and semiconductor intellectual property (IP) for Samsung's 14-nm FinFET process.

The Synopsys Galaxy™ Design Platform and DesignWare® IP have been successfully deployed on multiple SoC designs using the 14-nm FinFET process. The solution includes the Design Compiler® tool for area and power-efficient synthesis, a TetraMAX® solution for cell-aware ATPG, IC Compiler™ technology for DPT-aware and 14nm-ready place and route, IC Validator for fast physical verification, PrimeRail for accurate electro migration and IR drop analysis, the StarRC™ tool for 3-D extraction, and HSPICE® simulation for 3-D device simulations. In semiconductor IP, Samsung and Synopsys have collaborated to successfully tape out test chips and develop DesignWare Interface, Embedded Memory and Logic Library IP in Samsung's 14-nm FinFET processes. One example of the collaboration is the new DesignWare USB femtoPHYs, which reduce area by up to 50 percent compared to previous generations. The USB femtoPHYs are silicon-proven in Samsung's process and have passed USB-IF compliance testing.

"From the early research stage of our 14-nm FinFET process, we have had deep technology collaborations with Synopsys for design tools and IP," said Dr. Shawn Han, vice president of foundry marketing, Samsung Electronics. "The multiyear collaboration has resulted in silicon-proven solution that can enable Samsung foundry customers to achieve the maximum value from the latest FinFET processes. We will see the revolutionary 14-nm FinFET SoCs in our hands starting early next year."

The collaboration also includes library qualification for timing and pin accessibility, routing rule development with support for double patterning, timing signoff correlation and accuracy testing to SPICE; validation of Samsung golden scripts and implementation and qualification of multiple IP titles.

"Our long standing collaboration with Samsung foundry is focused on enabling our mutual customers to achieve predictable design closure using the latest process technology," said Bijan Kiani, vice president of marketing, Synopsys' Design Group. "With the comprehensive FinFET-ready Galaxy Design Platform and DesignWare IP, engineers can accelerate the development of innovative products needed to win in today's competitive and fast moving marketplace."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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