Synopsys Introduces DesignWare ARC Processors Optimized for Low-Power Embedded DSP Applications

New ARC EM5D and EM7D Cores Combine High-Efficiency Control and Signal Processing to Minimize Energy Use in Sensor, Voice and Audio Processing Applications

MOUNTAIN VIEW, Calif., May 29, 2014 /PRNewswire/ --

Highlights:

- ARC EM5D and EM7D Processors with an optional Floating Point Unit (FPU) are based on the new ARCv2DSP Instruction Set Architecture (ISA), which includes more than 100 new DSP instructions
- New cores are optimized for ultra low-power embedded DSP applications, consuming as little as 7 microwatts/MHz on typical 40-nanometer (nm) LP processes for energy-efficient signal processing of voice/speech, audio and sensor data
- ARC MetaWare Toolkit provides a rich DSP software library and C/C++ Compiler for easy and efficient development of DSP algorithms and applications

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced availability of the DesignWare® ARC® EM DSP Family of processors, which includes the ARC EM5D and EM7D processors designed for low-power embedded digital signal processing applications. The processors are implementations of the new ARCv2DSP instruction set architecture (ISA), an enhancement to the efficiency-optimized ARCv2 ISA with over 100 new DSP instructions for accelerating signal processing algorithms, including vector and complex MUL/MAC operations. The ARC MetaWare Development toolkit supports C-language DSP programming with fixed-point data types and operator overloading. ARC EM DSP processors are based on the RISC architecture of the EM processor family, providing the combination of efficient real-time control and DSP performance required for ultra low-power, always-on devices that process audio, voice and sensor data.

"Consumers increasingly expect fully integrated, high-quality speech and audio technologies in their mobile devices, driving the need for hardware and software solutions that can deliver efficient RISC and DSP performance at ever-lower power consumption levels," said Bernard Brafman, vice president of business development at Sensory, Inc. "The combination of Sensory's leading TrulyHandsfree™ technology and ARC EM DSP processors will enable our mutual customers to implement state-of-the-art voice activation capabilities in their products without compromising performance or battery life."

The ARC EM DSP processors implement a processing pipeline that offers an optimal balance of performance, power consumption and size for a wide range of control and DSP applications. The processor cores include a unified, single-cycle 32 x 32 MUL/MAC unit with 40-bit/72-bit accumulators. To deliver enhanced performance for filtering, fast Fourier transform (FFT) and other signal processing algorithms, the EM5D and EM7D feature fractional support (e.g., Q31 and Q15 data types) with saturating arithmetic, rounding and non-rounding instructions, as well as divide and square root. Vector support provides greater processor efficiency by enabling multiple data values to be processed in a single operation. The ARC EM5D and EM7D processors deliver excellent performance efficiency, consuming as little as seven microwatts/MHz in a typical 40-nm LP process technology. This high degree of performance efficiency makes the new cores ideally suited for 'always-on' voice activation in Internet-of-Things (IoT) applications. For example, Sensory Inc.'s TrulyHandsfree™ Voice Control software consumes less than four microwatts when executing Sensory's Low Power Sound Detection technology on an ARC EM5D processor implemented in a 28-nm HPM process (logic and memory dynamic power). This enables an integrated hardware-software solution for voice activation and control with ultra-low energy consumption. Like all ARC processors, EM DSP processors are highly configurable so that each instance can be tailored to achieve the optimum balance of DSP and RISC performance as well as power and area efficiency. In addition, ARC Processor EXtensions (APEX) technology allows designers to create user-defined instructions, enabling the integration of custom hardware accelerators that improve application-specific performance while reducing power consumption and the amount of memory required. The ARC processors' extensible architecture also helps minimize system-level latencies and silicon area by enabling memory and system-on-a-chip (SoC) peripherals to be directly connected to the processor for single-cycle access. Native ARM® AMBA® AHB™ and AHB-Lite™ as well as BVCI interfaces deliver efficient system throughput. An optional IEEE-754 compliant FPU supporting single- and double-precision operations is also available.

The DesignWare ARC MetaWare Development Toolkit is a complete solution for developing, debugging and optimizing embedded software targeted for ARC processors, including the new EM DSP processors. It includes an enhanced C/C++ compiler supporting the new DSP instructions for efficient algorithm development. The

toolkit also includes a DSP software library of fixed-point math functions and an instruction-accurate simulator that includes accurate modeling of the new DSP operations.

"There has been a rapid proliferation of feature-rich mobile and IoT electronics needing instantaneous responses to audible commands or movements," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "Addressing the needs of these low-power designs requires a processor that is highly efficient at processing both control and DSP tasks. The new ARC EM5D and EM7D processors extend the proven EM family with energy-efficient signal processing capabilities ideally suited for the growing number of always-on devices."

Availability and Resources

ARC EM5D and EM7D processors are scheduled for general availability in July. The associated development tools will be available in June.

- Learn more about the ARC EM DSP processors:http://www.synopsys.com/dw/ipdir.php?ds=arc-em-dsp

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor solutions and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

Editorial Contacts:
Monica Marmie
Synopsys, Inc.
650-584-2890
monical@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900, ext.114
sbrennan@mcapr.com

SOURCE Synopsys, Inc.