Synopsys and TSMC Collaborate to Validate DesignWare IP in TSMC 16-nm FinFET Process

Silicon Success of DesignWare USB 3.0 femtoPHY, Logic Libraries and Embedded Memories in TSMC 16-nm FinFET Process Verifies Robustness of Both IP and Process

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Highlights:

- Validated IP in TSMC 16-nm FinFET process accelerates 16-nm FinFET Plus (16FF+) IP development and reduces SoC integration risk
- Portfolio of IP under development for TSMC 16FF+ process includes DesignWare Interface, Logic Library and Embedded Memory IP
- TSMC 16-nm FinFET and 16FF+ processes significantly improve performance and lower power compared to planar technologies

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the validation of DesignWare® IP in the TSMC 16-nanometer (nm) FinFET process technology, demonstrating the ongoing collaboration between Synopsys and TSMC to provide designers with proven IP for their advanced system-on-chip (SoC) designs. The silicon success of the DesignWare USB 3.0 femtoPHY IP, Logic Libraries and Embedded Memories in TSMC's 16-nm FinFET process is evidence of both companies' deep expertise in delivering high-quality IP, enabling designers to integrate needed functionality with less risk and paving the way for the successful deployment of IP in TSMC's 16FF+ process. Designers developing SoCs in TSMC's 16-nm FinFET process can take advantage of the doubled transistor density, which reduces power consumption by up to 55 percent or increases performance by up to 35 percent compared to TSMC's 28-nm process.

Synopsys' DesignWare USB, Logic Library and Embedded Memory IP in TSMC's 16-nm FinFET process, combined with the DesignWare STAR Memory System® and DesignWare STAR Hierarchical System embedded test and repair solutions, enable designers to incorporate more functionality into advanced SoCs while meeting high performance, low power and small silicon area requirements. TSMC is using the STAR Memory System to test, repair and diagnose memories in all of its 16FF+ test chips.

The three-dimensional structure of FinFET devices represents a significant change in transistor manufacturing that significantly impacts IP design. Working closely with TSMC and leading customers enabled Synopsys to gain design expertise and a deep understanding of IP architectures. Synopsys' IP solutions for FinFET implement proven technologies to successfully manage the change from planar to 3-D transistors, including 16-nm FinFET and 16FF+. Furthermore, Synopsys provides TCAD and mask synthesis products used by foundries for FinFET process development.

"TSMC's longstanding collaboration with Synopsys has enabled us to offer designers access to a broad portfolio of high-quality IP solutions for a wide range of TSMC processes," said Suk Lee, TSMC Senior Director, Design Infrastructure Marketing Division. "Working with Synopsys on the development of the DesignWare Interface, Logic Library and Embedded Memory IP for TSMC's advanced 16-nm FinFET process extends our long history of success, and puts Synopsys on track to deliver quality IP in the 16FF+ process to reduce integration risk and accelerate time-to-volume production for our mutual customers."

Synopsys' DesignWare USB IP has been implemented in more than 3,000 designs and ported to more than 100 process technologies, giving designers immediate access to low-power, small area IP in their required process technology. The DesignWare Logic Libraries and Embedded Memories consist of a broad range of high-speed, high-density and low-power memories and standard cell libraries optimized for maximum performance with the lowest possible power consumption.

Synopsys has optimized the DesignWare STAR Memory System for memory test, repair and diagnostics and DesignWare STAR Hierarchical System for test integration and pattern re-use of all IP on an SoC for TSMC's 16-nm FinFET process. The hierarchical test and repair solutions enable designers and test engineers to increase test productivity, reduce overall test cost and improve test quality-of-results (QoR).

"Synopsys' close collaboration with TSMC has enabled us to successfully deliver silicon-proven IP in TSMC's advanced 16-nm FinFET process and help designers accelerate the adoption of FinFET technology for higher-performance and more power-efficient SoCs," said John Koeter, vice president of marketing for IP and systems at Synopsys. "The successful DesignWare IP silicon results, combined with the experience gained from developing IP for the 16-nm FinFET process, put us in a strong position to deliver on our 16FF+ roadmap,

enabling designers to gain the full benefits of the advanced node and bring differentiated products to market faster."

Availability

The DesignWare USB 3.0 femtoPHY IP, Logic Libraries and Embedded Memories, STAR Memory System and STAR Hierarchical System for TSMC's 16-nm FinFET process are available now.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and next-generation verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor solutions and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits and date of availability of the DesignWare PHY IP for the TSMC 28-nm process. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, engineering difficulties and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2010 entitled "Risk Factors."

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