Synopsys Unveils Industry's First Complete PCI Express 4.0 IP Solution

High-Quality DesignWare PHY, Controller and Verification IP for PCI Express Architecture Doubles Performance to 16 GT/s for Enterprise SoC Designs

MOUNTAIN VIEW, Calif., May 22, 2014 /PRNewswire/ --

Highlights:

- Industry's first complete PCI Express® 4.0 IP solution, supporting the latest PCI Express 4.0 standard, will be featured on June 4th at the PCI-SIG® Developers Conference 2014 inSanta Clara, Calif.
- Synopsys DesignWare® Controller IP for PCI Express 4.0 architecture provides port logic for endpoints, root complex, dual mode (endpoint/root complex) and switch applications with minimized latency, gate count and power consumption
- Verification IP for PCI Express 4.0 architecture will verify PCI Express endpoints, switch and root complex devices with software/firmware equivalent application layers that vastly simplify testbench development
- DesignWare PHY IP for PCI Express 4.0 architecture, currently in development, will offer advanced equalization capabilities to increase signal integrity at high speed data rates across legacy channels while offering optimized active and standby power
- Availability of high-quality IP with early support for the PCI Express 4.0 specification lowers integration risk and accelerates availability of devices incorporating the new 16 GT/s speed

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today introduced the industry's first complete PCI Express 4.0 IP solution, consisting of DesignWare PHY, controllers and verification IP (VIP) targeting enterprise computing applications such as servers, networking, storage systems and solid state drives (SSDs). The PCI Express 4.0 specification, the next generation of the PCI Express I/O standard, doubles throughput to 16 GT/s and is currently at a preliminary revision 0.3 within the PCI Special Interest Group (PCI-SIG). The DesignWare IP for PCI Express 4.0 architecture enables easy system-on-chip (SoC) integration of 16 GT/s performance and the power-saving features defined in the PCI Express 4.0 specification. Based on proven technology in the DesignWare IP for PCI Express 3.0, 2.1 and 1.1 architectures, which combined have more than 1,000 design wins, the DesignWare IP for PCI Express 4.0 architecture allows designers to quickly incorporate the new PCI Express 4.0 standard into their products with less risk and improved time-to-market.

"Synopsys is an aggressive, early supporter of the PCI Express 4.0 specification, which provides critical performance and power enhancements to high-end server and enterprise applications," said Bruce Tolley, vice president of technical and solutions marketing at Solarflare. "As the leader in application-intelligent Ethernet network interface software and hardware, we rely on Synopsys to provide us with trusted PCI Express IP solutions that support the latest specifications. Synopsys' early support of the PCI Express 4.0 specification, combined with the company's best-in-class technical support, is exactly what we expect from the leading provider of PCI Express IP."

"Teledyne-LeCroy has worked closely with Synopsys in the past to ensure interoperability and standards compliance for the PCI Express and M-PCIe™ specifications," said John Wiedemeier, product marketing manager at Teledyne-LeCroy. "To accelerate time-to-market, designers require a high-quality IP product that helps lower the risk of incorporating the interface into their SoCs. Our collaborative relationship with Synopsys on the latest PCI Express specifications strengthens the ecosystem for everyone and allows developers of enterprise SoCs to leverage proven solutions."

The DesignWare PHY IP for PCI Express 4.0 architecture will support full-featured bifurcation and aggregation, offering designers the flexibility either to configure the PHY macro into multiple individual links at 2.5, 5, 8 or 16 GT/s, or to aggregate the PHY macro up to 16 lanes. For increased signal integrity at high-speed data rates across legacy channels, the PHY analog front-end will include 5-tap DFE, continuous time linear equalization (CTLE) and feed forward equalization (FFE) with advanced algorithms for link initialization and adaptation. As power reduction is a key requirement in many markets, the DesignWare PHY IP will reduce both active and standby power consumption through advanced techniques including L1 sub-states. Support for Separate Refclk Independent SSC (SRIS) will allow the use of cables to enable a new class of PCI Express applications outside of the system.

The low-power, low-latency DesignWare Controller IP for PCI Express 4.0 architecture is backward compatible with the PCI Express specification (4.0, 3.0, 2.1, 1.1, M-PCIe and optional features including L1 sub-states) across Switch, Endpoint, Dual Mode and Root Complex port types, with support for embedded DMA and SR-IOV. ARM® AMBA® 4 AXI™, AMBA 3 AXI and AMBA AHB™ and native interfaces are available in the DesignWare Controller IP for PCI Express 4.0 architecture, as well as in previous generations, enabling designers to quickly upgrade to the PCI Express 4.0 technology. Based on existing

DesignWare IP architectures, the DesignWare Controller IP for PCI Express 4.0 architecture supports multiple lanes (x1 to x16) and multiple datapath widths, enabling an optimized solution for the target application while minimizing gate counts and reducing design risk.

The Synopsys Verification IP for PCI Express architecture will be available to thoroughly verify designs based on the PCI Express 4.0, 3.0, 2.1 and 1.1 specifications. It will be fully configurable to support verification of PCI Express technology endpoints, switches and root complex devices at the PIPE or serial interface. With this comprehensive set of protocol, methodology, coverage, verification and productivity features, designers will be able to achieve rapid verification closure of their designs using PCI Express technology.

"Enterprise applications require greater bandwidth through PCI Express interfaces to address the demands of servers, storage devices and switch interconnects," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "Synopsys is building on our leading PCI Express technology to enable designers to bring leading-edge products using the latest PCI Express specification to the market. Our complete DesignWare IP solution for the PCI Express 4.0 specification doubles performance over our existing PCI Express 3.0 IP, reduces design risk and accelerates time-to-revenue for designers implementing the PCI Express 4.0 architecture in their SoCs."

Availability

The DesignWare Controller IP for PCI Express 4.0 architecture is available now. Synopsys Verification IP for PCI Express 4.0 architecture is scheduled for early availability in Q3 2014. For availability information on DesignWare PHY IP for PCI Express 4.0 architecture in leading 14/16-nm FinFET and 28-nm process technologies, please contact Synopsys.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and next-generation verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor solutions and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

Editorial Contacts:
Monica Marmie
Synopsys, Inc.
650-584-2890
monical@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900, ext.114
sbrennan@mcapr.com

SOURCE Synopsys, Inc.