Synopsys DFTMAX Ultra Deployed By Dialog Semiconductor to Successfully Test Silicon Parts

Delivers 3X Higher Test Compression and Ease-of-Deployment

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Highlights:

- Dialog deployed DFTMAX Ultra on a mixed-signal IC in less than a day
- The device was manufactured and successfully tested for silicon defects
- Test time reduced by more than 3X

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that Dialog Semiconductor, a provider of highly integrated power management, audio, AC/DC and short-range wireless technologies, successfully deployed Synopsys' DFTMAX™ Ultra product on a mixed-signal test chip to lower manufacturing test costs. In today's competitive markets, lowering the cost of testing ICs is essential as IC providers move from early samples to high volume production. Built into Synopsys' Design Compiler® RTL synthesis and linked to Synopsys' TetraMAX® ATPG, DFTMAX Ultra was deployed on the design in a single day and delivered 3X higher time compression.

"Using DFTMAX Ultra, we implemented test compression into a mixed-signal design in just a few hours and successfully tested the manufactured parts," said Mark Tyndall, senior vice-president of Corporate Development and Strategy, general manager of the Power Conversion Business Group, Dialog Semiconductor. "We observed DFTMAX Ultra reduce test time by 3X and more compared to our previous compression technology and require few device pins."

Synopsys' DFTMAX Ultra efficiently streams compressed test data in and out of the design-for-test circuitry, significantly lowering the amount of data required to achieve high manufacturing test quality of silicon parts. The tool-generated architecture requires fewer test pins and enables silicon parts to operate at higher frequencies while in test mode. As a result, engineers can test more die in parallel and reduce the time required to test each die. For superior quality of results and faster turnaround time, DFTMAX Ultra is built into Design Compiler and linked with TetraMAX ATPG and the Synopsys Galaxy™ Design Platform suite of tools, concurrently optimizing for speed, area, power, test and yield.

"Success with DFTMAX Ultra on silicon parts underscores Synopsys' commitment to helping customers meet their most demanding test quality and cost requirements," said Bijan Kiani, vice president of marketing in Synopsys' Design Group. "State-of-the-art synthesis-based test technology in DFTMAX Ultra and tight links with the Synopsys Galaxy Design Platform enable design teams to lower test costs, increase test quality and accelerate design schedules."

About the Synopsys Synthesis-Based Test Solution

The Synopsys synthesis-based test solution is comprised of DFTMAX Ultra, DFTMAX and TetraMAX for power-aware logic test and physical diagnostics; DesignWare® STAR Hierarchical System for IEEE standards-based hierarchical SoC test; DesignWare STAR Memory System® for embedded and external memory test, repair and diagnostics; DesignWare IP for high-speed interfaces with self-test; Yield Explorer® design-centric yield analysis; and Camelot™ for failure analysis CAD navigation. Synopsys' test solution combines Design Compiler RTL synthesis with embedded test technology to optimize timing, power, area and congestion for test as well as functional logic, leading to faster time-to-results due to zero or minimal design iterations. The solution contains value links among the test products and across the Synopsys Galaxy Design Platform to enable faster turnaround time meeting both design and test goals, higher defect coverage and faster yield ramp.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys

technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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