Centaur Technology Deploys Synopsys' Formality Ultra to Shorten Design Schedules by Weeks

Enables 2X Faster Implementation and Verification of Functional ECOs

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Highlights:

- Formality Ultra accelerates functional ECO cycles leading to weeks of schedule savings
- Centaur Technology deploys Formality Ultra on its x86 compatible microprocessor designs

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that Centaur Technology, a subsidiary of VIA Technology, has deployed Synopsys' Formality® Ultra tool for implementation and verification of engineering change orders (ECOs), accelerating the design of its high-performance, low-cost x86 compatible designs. With new microprocessors going from concept to completion in about nine months, schedule predictability and fast ECO cycles are a must for Centaur Technology. Utilizing Formality Ultra, Centaur Technology is now able to complete each functional ECO in hours versus the days or even weeks required with traditional manual methods, significantly shortening design schedules.

"Having the fastest design cycle in the industry is one of our key competitive advantages and we continuously strive to accelerate it," said Mark Brazell, senior engineer at Centaur Technology. "With the adoption of Formality Ultra, we are able to implement functional ECOs much faster, shorten our schedule by weeks and increase our competitiveness in the marketplace. Formality Ultra is now an essential part of our design flow."

Formality Ultra includes advanced matching techniques that visually highlight the mismatch between the RTL and netlist representations of a design, efficiently pointing designers to the changes required to implement an ECO. In addition, a multi-point verification technology quickly checks changes made to the design enabling designers to verify the correctness of their ECOs in a matter of minutes on multimillion-instance designs. These capabilities can significantly reduce the time designers spend in the ECO implementation cycle, resulting in shorter, more predictable design schedules.

"Shorter design schedules are key to companies like Centaur Technology in the low-cost microprocessor markets, as well as other competitive markets," said Bijan Kiani, vice president of marketing, Design Group at Synopsys. "Formality Ultra enables designers to significantly reduce the time and effort required to implement functional ECOs, increase schedule predictability and shorten design time."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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