Synopsys' New ProtoCompiler Software Speeds Time to First Prototype by Up to 3X

Prototyping Automation and Debug Software for HAPS FPGA-based Prototyping Systems Improves Prototyping Performance

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Highlights:

- ProtoCompiler software and integrated HAPS hardware accelerate time to prototype bring-up and improve prototype performance
- Automated partitioning capability across multiple FPGAs decreases runtime from hours to minutes for up to 250 million ASIC gate designs
- Enables efficient implementation of proprietary pin multiplexing for 2X faster prototype performance on average
- Captures seconds of trace data with gigabytes of storage capacity for superior debug visibility

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of Synopsys' ProtoCompiler software for Synopsys' HAPS® FPGA-based prototyping systems. ProtoCompiler is an integrated prototyping tool set with built-in HAPS hardware knowledge, which enables the rapid bring-up of a prototype up to 3X faster than existing prototyping flows. ProtoCompiler also enables more efficient prototyping with HAPS by providing an automated partitioning engine, integrated debug support and improved HDL compilation.

ProtoCompiler enables designers to quickly compile RTL and then generate a multi-FPGA design partition in a matter of minutes, versus hours for an existing design flow. ProtoCompiler's high-capacity logic synthesis and partitioning features automatically generate a high-performance, cycle-accurate design representation that operates seamlessly across multiple FPGAs. The flow to convert ASIC RTL to HAPS multi-FPGA flexible architecture has been accelerated with multi-threaded processing, an optimized, faster compiler and ASIC gated clock-conversion methods tailored for the HAPS Series.

"Synopsys' HAPS FPGA-based prototyping is invaluable for accelerating hardware/software validation, helping us deliver our new OWL series tablet SoCs with higher quality and in less time," said Mu Wu, deputy manager, system verify department at Actions Semiconductor. "We are excited by the announcement of Synopsys' ProtoCompiler software, which will transform prototyping by providing automation and debug tools that have intimate knowledge of HAPS systems. This enables designers to achieve faster time to results with higher performance prototypes."

ProtoCompiler understands the HAPS hardware interconnect architecture and detailed trace delay timing information to enable automated multiplexing. The new tool capabilities combined with HAPS high-speed time-domain multiplexing (HSTDM) and Synopsys' HapsTrak® connectors enable an increased average of 2X system performance when compared to other solutions.

"The combination of Synopsys' ProtoCompiler software and Xilinx® Vivado® Design Suite's next-generation analytical place and route technology provides maximum productivity for design teams who prototype SoC designs with Synopsys HAPS and the Xilinx Virtex-7 FPGA family," said Tom Feist, senior marketing director of design methodology at Xilinx. "Designers using FPGAs for ASIC and SoC prototyping require rapid system bring-up and high-performance implementations, and ProtoCompiler's design automation and debug delivers on both of these requirements."

ProtoCompiler provides a range of design visibility features including simulator-like RTL debug, automated connection to logic analyzers, full visibility with Synopsys' Siloti® visibility automation technology and superior debug and analysis with the Synopsys Verdi3™ automated debug environment to troubleshoot tasks throughout the prototype's lifecycle. Greater visibility into a multi-FPGA HAPS system is enabled by RTL instrumentation, gigabytes of sample trace storage and a non-invasive approach to the prototype-to-workstation connection that does not consume general purpose FPGA I/Os. Gigabyte storage options provide full seconds of debug visibility essential for the validation of complex hardware/software interactions. ProtoCompiler debug capabilities also integrate with the functional verification capabilities of Synopsys' Verification Compiler™ flow to deliver comprehensive visualization across static, formal, simulation, VIP, emulation and prototyping.

"Prototype designers have a short period of time between the 'RTL-drop' and delivery of an operational prototype for hardware/software integration. ProtoCompiler's HAPS-aware capabilities enable developers to accelerate their time to first prototype, while providing significant debug capacity and high system performance," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "Our integrated hardware/software solution using ProtoCompiler and HAPS gets prototypers up and running much faster and with better results than traditional methods."

Availability & Resources

ProtoCompiler software is available now and compatible with HAPS-DX and HAPS-70 Series systems. A variant of ProtoCompiler, ProtoCompiler DX, is included with all HAPS-DX systems.

Learn more about ProtoCompiler:

- ProtoCompiler: https://www.synopsys.com/protocompiler
- FPGA-based Prototyping Methodology Manual: https://www.synopsys.com/FPMM
- FPGA-based Prototyping blog: https://blogs.synopsys.com/breakingthethreelaws/
- HAPS-70 Series: https://www.synopsys.com/haps70
- HAPS-DX Series: https://www.synopsys.com/haps-dx

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at https://www.synopsys.com.

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