Synopsys Announces Industry's First Complete LPDDR4 IP Solution for High-Performance, Low-Power Mobile SoC Designs

PHY, Controller and Verification IP Deliver up to 3200 Mbps Speeds for High-End Smartphones and Tablets

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Highlights:

- Supports LPDDR4 up to 3200 Mbps with low power consumption
- Backward compatibility with LPDDR3 and DDR3/4 SDRAMs simplifies design transition from one SDRAM standard to the next
- Package-on-package (PoP) support reduces PCB area in smartphones, while memory-on-PCB support allows for bandwidth and capacity expansion for tablets, notebooks and ultraportable laptops
- Complete LPDDR4 IP solution includes LPDDR4 multiPHY with I/Os, Enhanced Universal DDR Memory Controller and verification IP, as well as hardening and signal integrity services, to ease integration and accelerate time-to-market
- The LPDDR4 IP solution is built on Synopsys' extensive experience supporting more than 800 customer design wins over the past 15 years

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today introduced the industry's first complete LPDDR4 IP solution, which includes Synopsys' DesignWare® LPDDR4 multiPHY, Enhanced Universal DDR Memory Controller (uMCTL2) and verification IP (VIP), as well as hardening and signal integrity services. Synopsys' DesignWare LPDDR4 IP solution supports all key LPDDR4 features, including up to 3200 Mbps performance and features to reduce power consumption, delivering a low-power memory solution for mobile and graphics-intensive system-on-chips (SoCs).

"LPDDR4 technology enables new, lower power mobile devices with higher graphics capabilities that deliver an immersive and exhilarating user experience," said Dan Skinner, director of DRAM architecture at Micron Technology. "Micron is leading the way on this new mobile memory technology and our customers will be first to market with the help of Synopsys, which is providing early availability of a complete LPDDR4 IP solution before the standard is finalized. Together we're building a LPDDR4 ecosystem to jump-start these innovative, mobile designs."

The DesignWare LPDDR4 IP solution supports data rates up to 3200 Mbps to meet the demands of faster processors, high-resolution displays, HD video and graphics-intensive games in mobile SoC applications. Fast frequency switching matches memory bandwidth to the device workload to optimize performance and power consumption. The DesignWare LPDDR4 IP solution can reduce power consumption per bit transferred by incorporating multiple power-saving features such as low-power modes (including power-down, self-refresh, and deep power-down), clock gating and power down of sections of the PHY that are not in use at a given moment. These features can extend the battery life of mobile devices and support consumers' increasing requirements for thin and light devices.

To minimize design risk, the DesignWare LPDDR4 IP solution includes backward compatibility with LPDDR3 and DDR3/4 SDRAMs to simplify the design transition from one SDRAM standard to the next. In addition, the LPDDR4 IP supports a split PHY implementation to permit designers to distribute the IP

around the SoC, optimizing the interface for area-efficient PoP assembly and offering a low-risk evolutionary path from previous-generation mobile memories. Designers can take advantage of Synopsys' DDR hardening and signal integrity services to harden the LPDDR4 multiPHY and to analyze the signal integrity of the entire system (silicon, package and PCB), easing IP integration and reducing potential risks in the use of advanced manufacturing technologies.

"Synopsys is focused on providing IP on the leading edge of both functionality and process," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "The LPDDR4 solution announced today builds upon our 15 years of experience in the DDR IP space as well as our experience with customers successfully implementing DesignWare DDR IP in their SoCs and electronic systems."

Availability

The DesignWare Enhanced Universal DDR Memory Controller IP with support for LPDDR4 is available now. The DesignWare LPDDR4 multiPHY IP is scheduled to be available in Q3 2014 in a leading 16-nm FinFET process technology. Verification IP for LPDDR4 is scheduled for early availability in Q3 2014.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and next-generation verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor solutions and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits and date of availability of the DesignWare LPDDR4 multiPHY IP for 16-nm FinFET process technology and verification IP for LPDDR4. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen production or delivery delays, failure to perform as expected, product errors or defects and other risks identified in the "Risk Factors" section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended January 31, 2014.

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