

# TSMC Certifies Synopsys Digital and Custom Solution for V1.0 N16 Process

Certification Enables Designers to Realize the Power, Performance and Area Benefits of FinFET Technology

MOUNTAIN VIEW, Calif., April 14, 2014 /PRNewswire/ --

## Highlights:

- Certification enables custom and cell-based designs deployed by early adopters
- Cell-based solution includes Design Compiler® synthesis, IC Compiler™ physical implementation, IC Validator physical verification, StarRC™ extraction and PrimeTime® timing analysis
- Custom solution includes HSPICE® circuit simulation, FastSPICE simulation with CustomSim™ and FineSim® tools, static timing analysis with NanoTime and custom implementation with the Laker® solution

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced immediate availability of the V1.0 certified solution for cell-based and custom implementation with the TSMC N16 FinFET process. The TSMC-certified solution delivers predictable design closure with production-ready FinFET design automation tools. It allows engineers designing the next wave of semiconductors to deliver faster, more power-efficient and denser chips. Details of Synopsys' FinFET solution can be found at [www.synopsys.com/finfet](http://www.synopsys.com/finfet).

"Delivering innovations to bring out the best of every new process technology has been a key focus of the longstanding collaboration between TSMC and Synopsys," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division. "Given the complexity of dealing with 3-D transistors, we started early and significantly broadened our collaboration with Synopsys to deliver on the promise of FinFET technology. With the availability of V1.0 certified tools, all our customers can now realize the full potential of FinFET technology."

"The V1.0 certification of our Galaxy Design Platform for the N16 FinFET process is the result of many innovations realized through the deep engineering collaboration between TSMC and Synopsys," said Bijan Kiani, vice president of marketing for the Design Group at Synopsys, Inc. "We worked with TSMC and our mutual customers across multiple market segments to deliver a complete, efficient and proven flow. This allows engineers to make the most of FinFET technology and deliver state-of-the-art designs."

## About the TSMC N16 V1.0 Certified Solution

Synopsys' Galaxy™ Design Platform provides comprehensive tools and methodology support for customers designing with TSMC's 16-nm FinFET process:

- IC Compiler: Advanced technology supports 16-nm FinFET quantized rules, FinFET grid rules and advanced optimization methodology, including PBA vs. GBA timing correlation and low-voltage hold time fixing to achieve optimal performance, power and area
- IC Validator: DRC and DPT rule compliance checks verify FinFET parameters, including fin boundary rules and expanding dummy cells
- PrimeTime: Advanced waveform-propagation delay calculation delivers static timing analysis (STA) signoff accuracy required for FinFET processes
- StarRC: Pioneering "real profile" FinFET device modeling provides precise middle-end-of-line (MEOL) parasitic extraction for accurate transistor-level analysis

- HSPICE, CustomSim and FineSim: FinFET device modeling and accurate circuit simulation for the latest FinFET-based designs. In addition, CustomSim delivers new capabilities for electromigration and IR-drop analysis
- Laker: Support for complex FinFET abutment rules, double-patterning, MEOL layers and other advanced-node design requirements

### **About Synopsys**

Synopsys, Inc. (Nasdaq: SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at [www.synopsys.com](http://www.synopsys.com).

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