Synopsys Unveils IC Compiler II, Enabling a Game-Changing, 10X Increase in Physical Design Throughput

Industry Leaders Collaborate with Synopsys to Bring New Technology into Production Use

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Highlights:

- 10X faster design planning, 5X faster implementation, 2X larger capacity – all lead to 10X faster throughput
- Built on completely new scalable infrastructure, timer and analytical optimization engines
- Already contributing to production tapeouts at established and emerging technology nodes

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today unveiled IC Compiler II, a game-changing successor to its IC Compiler™ product, the industry's current leading place-and-route solution for advanced design at both established and emerging nodes. Built from the ground up on a completely new, multi-threaded infrastructure, IC Compiler II introduces ultra-high-capacity design planning, unique clock-building technology and advanced global-analytical closure techniques. IC Compiler II ushers in a new era of productivity by enabling a 10X increase in physical design throughput and is already contributing to successful tapeouts at leading customers. Several of these customers will be sharing their experiences with IC Compiler II at the Synopsys Users Group (SNUG) Silicon Valley, opening at the Santa Clara Convention Center. See what early partners experienced with IC Compiler II

"From RTL synthesis to static timing to physical synthesis, Synopsys has a history of innovations that have transformed electronic design. With IC Compiler II, we are approaching another transformative juncture," said Antun Domic, executive vice-president and general manager of the Design Group at Synopsys. "Built from scratch for speed, and incorporating newly developed algorithmic approaches, this new solution offers un-paralleled improvements in throughput, opening the door to a world of new possibilities in physical design."

Synopsys' IC Compiler has long been recognized as the winning choice for advanced, high-performance designs at emerging, as well as established, silicon technology nodes. While continuously investing to ensure that IC Compiler remains state of the art, several years ago, Synopsys began building a new place-and-route system aimed at providing an order-of-magnitude leap in designer productivity. This massive undertaking has been made possible by an asset mix unique to Synopsys: a deep resource pool to sustain parallel development efforts, advanced technical expertise to pursue fundamental advances in core algorithms and broad customer collaboration to provide feedback and to refine the new technology through use in actual designs. The result of this initiative is Synopsys' newest place-and-route solution, IC Compiler II. Synopsys will continue to enhance and support IC Compiler, providing flexibility for customers who wish to continue using it, and offering the possibility to move up to IC Compiler II at a time of their choosing.

IC Compiler II is a full-featured place-and-route system centered on a new multi-threaded infrastructure able to handle designs with more than 500 million instances. Exemplifying its "rethink, rebuild and reuse" development strategy, IC Compiler II relies on industry standard input and output formats, as well as familiar interfaces and process technology files, while introducing innovative design storage capability. It was architected with a full chip-level focus from day one, deploying novel design planning capabilities that provide a 10X performance boost while consuming 5X smaller memory. This enables designers to quickly evaluate many floor-planning alternatives to arrive at the right starting point for implementation. Complementing these chip-level capabilities is the block-level functionality powered by a new global-analytical optimization engine, a completely new clock generator and unique algorithmic capabilities in post-route optimization, which together enable enhanced quality of results (QoR) in area, timing and power. IC Compiler II also incorporates leading technologies used in IC Compiler, such as the conjugate-gradient placer and the ZRoute router. IC Compiler II achieves its results with an average of 5X faster runtime and 2X reduction in memory over the current solution. The combination of runtime speed-ups, superior floor plans, achievable QoR and an efficient, lightweight environment enable a reduction in design iterations, further boosting design productivity.

IC Compiler II has been built in close collaboration with some of the world's leading design groups. Initial shipment starts in mid-2014.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers

address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

Forward-looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934 regarding the expected release and benefits of IC Compiler II. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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