MediaTek Embarking On Deployment of Synopsys IC Compiler for Hierarchical Design Implementation

Successful Collaboration on Design Planning Automation is a Pivotal Contributor

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Highlights:

- MediaTek is deploying IC Compiler extensively for hierarchical system on a chip (SoC) design
- Close collaboration on hierarchical design planning technologies and methodology is key to success
- Enabling technologies in IC Compiler include data flow analysis, large design handling, support for multiple instantiated blocks, and Design Compiler Graphical flow

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that MediaTek Inc., a leading fabless semiconductor company for wireless communications and digital multimedia solutions, has initiated deployment of Synopsys' IC Compiler™ place and route solution for hierarchical design implementation. Already in use for block implementation at MediaTek, this successful collaboration extends the deployment of IC Compiler to the full flow starting from hierarchical design planning, through top and block-level place and route to final chip assembly.

"MediaTek is a pioneer in the rapidly evolving mobile multimedia space, delivering unbeatable performance and power efficiency at an affordable cost," said Andrew Chang, Corporate Vice President, MediaTek, Inc. "Our excellent experience with IC Compiler on some of our very complex chips and the close partnership with Synopsys has convinced us to extend the usage to our hierarchical designs."

As the largest chip set supplier for the midrange smartphone and tablet market, MediaTek is focused on enabling customers to deliver premium products at an attractive price point. Characterized by longer battery life, fast processing times and fully-featured multimedia support, MediaTek chipsets include industry leading processor and graphics cores along with the latest in multiprocessing and wireless communications technology. To deliver these sophisticated chipsets and meet time to market windows, MediaTek wanted a predictable flow with fast turnaround times that could realize a design in the smallest area possible, with the lowest power and with blazingly fast performance. Having experienced firsthand the benefits of using IC Compiler at the block-level, MediaTek embarked upon a comprehensive collaboration to develop a hierarchical implementation methodology that would extend these benefits to SoC design. MediaTek's hierarchical implementation methodology with IC Compiler utilizes several key technologies including:

- Data flow analysis for improved macro placement
- Automatic support of multiple instantiated blocks
- UPF-based hierarchical partitioning
- Predictable flow starting from Design Compiler® Graphical

"As one of the fastest growing companies in the mobile platform space, MediaTek's success is marked by the innovative products they have introduced to their customers," said Antun Domic, executive vice president and general manager, Design Group at Synopsys. "The decision to rely on IC Compiler for block as well as hierarchical design is an excellent testimonial to our close collaboration and the strength of IC Compiler to meet their challenging design needs in a timely manner."

MediaTek will present on this topic during Synopsys User Group (SNUG) on Tuesday, March 25, 2014.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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