Synopsys Introduces Verification Compiler to Enable 3X Productivity

Delivers next-generation software technologies for complete verification flow

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Highlights:

- Next-generation verification technologies, including static and formal verification, provide 5X performance improvement
- Native integration of simulation, static and formal verification, verification IP (VIP), debug, and coverage technologies into a single product boosts performance and productivity
- New advanced SoC debug capabilities built on the easy-to-use Verdi^{3}™ debug platform enhance debug efficiency
- Complete low power verification with native low power simulation, X-propagation simulation, next generation low power static checking and low power formal verification
- A broad portfolio of VIP including ARM® AMBA® 4 AXI™ and AMBA 5 CHI interconnect, Ethernet, MIPI, PCIe and more, integrated with simulation and debug for highest performance and productivity
- Concurrent verification licensing enables 3X productivity improvement overall

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of Verification Compiler™ solution, a new product that represents a compelling vision in the industry for system-on-chip (SoC) verification technology and verification roadmaps. Verification Compiler is a complete portfolio of integrated, next-generation verification technologies that include advanced debug, static and formal verification, simulation, verification IP and coverage closure. Together these technologies offer a 5X performance improvement and a substantial increase in debug efficiency, enabling SoC design and verification teams to create a complete functional verification flow with a single product. The combination of next-generation technologies, integrated flows and a unique concurrent verification licensing model enables Verification Compiler to deliver 3X productivity overall – directly addressing the growing SoC time-to-market challenge.

"Verification complexity is continuing to grow at faster than Moore's law rates," said Jonah Alben, senior vice president of GPU Engineering at NVIDIA. "To cope with this, the industry needs next-generation verification technologies such as static and formal, along with better integrated flows that reduce the cost of investment in diverse verification approaches. Synopsys' Verification Compiler offers a vision with the potential to address these needs and take verification productivity to the next level, while continuing to promote open interfaces that enable industry innovation."

"Verification Compiler offers a new vision for verification," said Anil Jain, corporate vice president of engineering at Cavium. "We are facing an inflection point in verification, and our belief is that the remedy has to come not only from new technologies and substantial integration, but also from innovative access models that offer all technologies that are needed in a SoC verification flow. With Verification Compiler, Synopsys is delivering a product that finally makes that vision a reality."

"Altera SoCs are some of the most highly integrated, heterogeneous computing platforms in the industry, combining multi-core ARM processor systems, floating point DSP blocks, high-bandwidth I/O and high-performance programmable logic on a single die," said Ty Garibay, vice president of IC engineering at Altera Corporation. "As we migrate our SoCs to a third-generation 64-bit architecture integrated on Intel's 14 nm Tri-Gate process, the design and verification tools we use must operate and communicate seamlessly, giving us the ability to simulate and debug across the RTL, UVM and embedded software domains with a unified compiler and debugging flow. The introduction of Verification Compiler is an important step towards enabling our design teams to significantly improve our productivity."

Advanced Technology Required for SoC Verification

With mobile and the Internet-of-Things driving electronics growth, advanced SoC development faces exponential growth in verification complexity, new power efficiency requirements, increasing software content and tougher time-to-market pressures. Achieving verification closure for these complex SoCs requires a broad set of technologies including advanced debug, static and formal verification, low-power verification, verification IP and coverage closure.

To address this challenging verification landscape, Verification Compiler features a comprehensive set of next-generation technologies, including formal verification, SoC connectivity checking, SoC-scale clock domain

crossing (CDC) checking, X-propagation simulation, native low power simulation, and advanced verification planning and management. Verification Compiler also includes the entire portfolio of Synopsys' next-generation verification IP, including the corresponding test suites, all integrated for advanced debug and high-performance simulation. By integrating these technologies in a single product, Verification Compiler enables SoC design and verification teams to better solve the growing technical and schedule challenges of SoC verification.

Next-Generation Static and Formal Verification

Verification Compiler addresses the sheer capacity challenges of verifying complex SoCs with a next-generation static and formal verification technology that is 3X to 5X higher in performance and capacity compared to other solutions available today. This new technology includes formal property checking, low power static checking, CDC checks, SoC connectivity checks, advanced lint and sequential equivalence checking. Verification Compiler static and formal capabilities are fully compatible with the Synopsys Design Compiler® and Synopsys IC Compiler™ use model and flows.

Increased Debug Efficiency

Verification Compiler's debug capabilities are built using technology from Synopsys' Verdi^3, the industry's de-facto debug platform. Verification Compiler uses all of Verdi^3's latest debug technology including numerous innovative debug capabilities that offer substantially increased debug efficiency. These new capabilities include Interactive Testbench (UVM-aware) Debug, Transaction Debug, HW/SW Debug, Power-Aware Debug, and Protocol-Aware Debug, all built on a unified, consistent and easy-to-use environment. Verification Compiler further adds substantial debug efficiency through the tight integration of these advanced debug capabilities with simulation, VIP, formal verification, and coverage.

The Synopsys Verdi^3 debug platform continues to be available as a standalone product. Verdi^3 is an open platform enabling integration with other verification flows through the Fast Signal Data Base (FSDB) database as well as through Verdi Interoperability Apps (VIA). Accordingly, Verdi^3 will continue to fully support major simulation, emulation, and formal verification products in the market.

Concurrent Verification

Today's SoC verification flows require simultaneous use of various verification technologies by multiple teams across geographies. Furthermore, different points of the flow require different concentrations of technologies. These types of access bottlenecks greatly impact verification efficiency, cost and time-to-market. To address these bottlenecks, each Verification Compiler license includes three independent, concurrent keys: one key for all static and formal technologies; one key for simulation-related technologies (including all VIP); and one key for all debug technologies. These three keys can be used concurrently by a single user to enhance individual productivity, or they can be used independently by different individuals in the same company. This flexibility enables design teams to simultaneously perform multiple verification functions, achieving dramatic verification productivity improvements.

"We have been collaborating closely with many of our customers on their most complex verification challenges for many years," said Manoj Gandhi, senior vice president and general manager, Verification Group at Synopsys. "Over the past few years, we've built a strong portfolio of leading-edge verification software technologies. Verification Compiler takes these technologies to the next level by integrating them into a single product with unmatched performance, capabilities, and productivity, and lays the groundwork for even more advances in the future."

Availability

Verification Compiler is available now under limited customer availability, with general availability planned for December 2014.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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