CEVA Utilizes Synopsys' Design Compiler Graphical to Achieve Higher Frequency and Smaller Area for its DSP Cores

Expedites CEVA's Implementation of its DSPs by Simplifying the Back-end Flow with Highly Predictable Results

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Highlights:

- Predictable flow with minimum iterations through tight correlation with Synopsys' IC Compiler™ place-and-route solution
- Delivers 5 percent higher frequency and 7 percent smaller area

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems today announced that CEVA, Inc. (NASDAQ:CEVA), a leading licensor of silicon intellectual property (SIP) DSP cores and platform solutions, has utilized Synopsys' Design Compiler® Graphical RTL synthesis solution to accelerate the implementation of its DSP cores and achieve better power/performance/area (PPA) results. CEVA develops a range of application-specific cores for high-performance wireless and multimedia solutions where time-to-market and design goals are extremely challenging. Utilizing Design Compiler Graphical, a key component of Synopsys' Galaxy™ Implementation Platform, CEVA and its customers attain superior quality of results and shorter design schedules.

"With Design Compiler Graphical we were able to achieve 5 percent higher frequency and 7 percent smaller area," said Menachem Stern, vice president of research and development at CEVA. "Moreover, the tight correlation to IC Compiler helps reduce uncertainty and expedites the entire development flow. Use of Design Compiler Graphical offers our customers the ability to differentiate their advanced SoCs where performance and schedule are keys to achieving success in the highly competitive consumer electronics market."

Design Compiler Graphical advanced logical and physical optimizations help designers meet their challenging timing, area and power goals. In addition, Design Compiler Graphical provides physical guidance to IC Compiler, leading to tight correlation with post layout results and up to 1.5X faster placement runtimes. Design Compiler Graphical also enables RTL designers to address routing congestion and perform floorplan exploration prior to physical implementation, streamlining the flow and reducing iterations. By delivering superior results and predictable flow, Design Compiler Graphical addresses the needs of today's most difficult designs at both advanced and established nodes.

"Design Compiler Graphical is enabling companies like CEVA and its customers to meet the requirements of the most advanced wireless and multimedia applications," said Bijan Kiani, vice president of marketing in Synopsys' Design Group. "With its innovative synthesis technologies and tighter links to IC Compiler, Design Compiler Graphical has become the RTL synthesis solution of choice for designers worldwide."

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

About CEVA
CEVA is the world's leading licensor of silicon intellectual property (SIP) DSP cores and platform solutions for the mobile, portable and consumer electronics markets. CEVA's IP portfolio includes comprehensive technologies for cellular baseband (2G / 3G / 4G), multimedia (vision, imaging and HD audio), voice processing, Bluetooth, Serial Attached SCSI (SAS) and Serial ATA (SATA). In 2012, CEVA's IP was shipped in over 1.1 billion devices, powering smartphones from many of the world's leading OEMs, including HTC, Huawei, LG, Nokia, Motorola, Samsung, Sony, TCL and ZTE. Today, more than 40% of handsets shipped worldwide are powered by a CEVA DSP core. For more information, visit www.ceva-dsp.com. Follow CEVA on twitter at www.twitter.com/cevadsp.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

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