Synopsys Announces Immediate Availability of Multiprotocol DesignWare Enterprise 12G PHY IP

High-Performance PHY IP Supports 1.25 Gbps to 12.5 Gbps Throughput and Cuts Power Consumption by up to 20 Percent for High-End Networking and Computing Applications

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Highlights:

- Support for 1.25 Gbps to 12.5 Gbps data rates covers a broad range of protocols, including PCI Express® 3.0, SATA 6G, 10GBASE-KR, 10GBASE-KX4, 1000BASE-KX, CEI-6G/11G, SGMII, QSGMII, SFF-8431, CPRI, OBSAI and JESD204B
- Superior signal integrity across lossy backplanes and port side interfaces enabled by a high-performance analog front-end
- Up to 20 percent lower active and standby power consumption compared to competing solutions due to L1 sub-states support, novel transmitter design, DFE bypass and half-rate architecture
- Separate Refclk Independent SSC (SRIS) , reference clock sharing, and on-die test features improve system design and efficiency

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of its multiprotocol DesignWare® Enterprise 12G PHY IP to reduce power consumption and increase performance in a broad range of high-end networking and computing applications. Architected to address designers' growing performance/power trade-off challenges, the DesignWare Enterprise 12G PHY enables designers to easily integrate enterprise protocols, including PCI Express 3.0, SATA 6G, 10GBASE-KR, 10GBASE-KX4 (XAUI), 1000BASE-KX, CEI-6G/11G, SGMII, QSGMII, SFF-8431, CPRI, OBSAI and JESD204B, into their system-on-chips (SoCs) with higher performance and up to 20 percent lower power consumption than competing solutions.

The DesignWare Enterprise 12G PHY includes architectural innovations to significantly reduce power consumption for enterprise SoCs. The high-performance analog front-end incorporates power saving features in both active and standby modes of operation. The hybrid transmit drivers support low power voltage mode and high swing current mode, along with other power-reducing features such as L1 sub-states, optional I/O supply under drive and decision feedback equalization (DFE) bypass mode.

The high-performance DesignWare Enterprise 12G PHY supports chip-to-chip, backplane and port-side interfaces to enable complex system integration. The flexible Clock Multiplier Unit (CMU) includes multiple PLLs to transmit high-quality data from 1.25 Gbps to 12.5 Gbps across the long and lossy backplanes found in the most demanding applications, including legacy systems. The analog front-end includes 5-tap DFE, continuous time linear equalization (CTLE) and Feed Forward Equalization (FFE) with advanced algorithms for start-up and mission mode adaptation to enhance signal integrity in high throughput communication channels. The multi-lane architecture with other advanced features like reference clock forwarding and PCI Express aggregation and bifurcation gives designers a flexible, scalable PHY IP solution for high-speed SoCs.

"As a PCI-SIG member for more than a decade, Synopsys has played a valued role in the development of PCIe technology," said Al Yanes, PCI-SIG Chairman and President. "Its support of the PCIe 3.0 architecture helps enable the continued success of the PCI Express ecosystem."

"With the latest data center and cloud computing trends, such as software defined networking and low power microservers, system architects are increasingly implementing multiple high-bandwidth protocols in a single SoC," said John Koeter, vice president of marketing for IP and systems at Synopsys. "With the addition of the DesignWare Enterprise 12G PHY IP to our broad data center IP portfolio, we can help designers better address performance and power concerns in new cloud computing architectures."

Availability

The DesignWare Enterprise 12G PHY IP is available now for 28-nanometer (nm) process technologies with 14/16-nm FinFET in development. Synopsys' DesignWare IP portfolio for data centers also includes solutions for 40G/10G/1G Ethernet, DDR4/3, PCI Express 3.0/2.0, USB 3.0/2.0, SATA 6G and the ARM® AMBA® AXI4™ and AMBA 3 interconnect; logic libraries and embedded memories; and Synopsys ARC® processors, all of which are available now.

About DesignWare IP
Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries and configurable processor cores. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to following traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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