Fujitsu Semiconductor and Synopsys Deliver an Optimized and Predictable Customized SoC (ASIC) Design Flow

Design Compiler® Early Exploration, Complemented with New Algorithms for Area and Timing Optimization, Improves Design Utilization and Accelerates Time-to-Market

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Highlights:

- Early design exploration accelerates creation of high-quality RTL and floorplan
- Monotonic area optimization improves design utilization and lowers power consumption
- Placement- and congestion-aware synthesis enables a convergent handoff flow
- New predictable flow expedites final layout

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced, through joint collaboration with Fujitsu Semiconductor Limited, a faster, area-optimized and highly predictable Customized SoC (ASIC) design flow for mutual customers. Early exploration and consideration of physical data during synthesis are becoming important for Customized SoC designs to minimize unexpected iterations. The newly announced flow includes early design exploration with DC Explorer to accelerate first netlist handoff. Monotonic area optimization technology improves area and leakage power while maintaining timing results. The physically aware synthesis technology delivers a highly optimized netlist that is tightly correlated to final layout, providing early insights and minimizing iterations. This new flow, in collaboration with Fujitsu's innovative design planning technology, allows users to implement up to 33 percent more logic in the same die area, expedites the final layout process and enables mutual customers to bring competitive products to market faster, while minimizing schedule risk.

"It is critical that we provide our Customized SoC users an optimal flow to meet their design requirements," said Akihiro Yoshitake, general manager of Technology Development Center at Fujitsu Semiconductor. "Adding Design Compiler's early design exploration and innovative physically aware synthesis to our Customized SoC flow accelerates collaboration between logical and physical design. We can achieve a 33 percent design density improvement with this new flow, enabling customers to implement more functionality, which is critical for developing advanced and low power SoCs."

Design exploration enables identification of issues and faster "what-if" analyses early in the design flow, accelerating creation of high quality design data and providing a better starting point for synthesis. The new monotonic area optimization engine improves utilization while lowering leakage power. The advanced placement and congestion aware synthesis generates a routing-friendly netlist, leading to fewer iterations between synthesis and place and route for faster design closure. Design teams across multiple market segments are benefiting from these advancements and shortening their design schedules.

"Leading Customized SoC suppliers like Fujitsu are recognizing the value of a highly predictable flow for them and their customers," said Antun Domic, executive vice president and general manager of Synopsys' Design Group. "This new handoff flow will help Fujitsu and their customers accelerate design schedules while meeting aggressive design goals."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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