Synopsys New Ultra Low-Power Non-Volatile Memory IP Cuts Power by 90 Percent and Size in Half

DesignWare Multiple-Time Programmable NVM IP Reduces System Costs for Wireless and RFID / NFC Tag Applications

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Highlights:

- Synopsys DesignWare AEON Multiple-Time Programmable Ultra Low-Power Non-Volatile Memory IP optimized for power- and area-sensitive wireless applications and RFID / NFC tags
- Single-bit read capability and read operation down to 0.9V reduce power consumption by up to 90 percent compared to previous generation
- 50 percent area reduction over previous Synopsys NVM IP reduces overall system cost by reusing the system's existing analog blocks
- Support for up to 100,000 programming cycles allows RFID and NFC tags to be reused many times
- Fast programming mode reduces factory programming time by up to 70 percent

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of its DesignWare® AEON® Multiple-Time Programmable (MTP) Ultra Low-Power (ULP) Non-Volatile Memory (NVM) IP, optimized for the stringent power and area requirements of wireless and RFID/NFC ICs. The DesignWare AEON MTP ULP NVM IP cuts power consumption by up to 90 percent compared to the previous generation by offering a single-bit read capability, read operation down to 0.9V and peak current under 10uA during erase and programming. Reducing power consumption extends battery life in mobile systems, increases RFID/NFC tag sensitivity and reduces tag size by allowing the use of smaller antennas.

"The power and area reductions in Synopsys' ULP NVM IP enable us to maintain our strong position as a turn-key solution provider in the UHF RFID tag IC market," said Murilo Pessatti, CEO at Chipus. "As an analog IP company competing in the quickly evolving RFID market, we need reliable IP partners, and Synopsys has IP quality and support that we can trust. Based on our previous success using DesignWare NVM IP, we are confident that Synopsys' ULP NVM IP will enable us to continue to build competitive products that meet our customers' power and area demands."

"Offering ULP NVM IP on our high-volume 180 nanometer CMOS process will enable our customers to reduce their overall system costs and meet the ultra low-power requirements of RFID and NFC tags," said Yit Loong Lai, senior vice president at SilTerra. "DesignWare NVM IP aligns well with our process technology to deliver an ideal combination of density, speed, and enduring performance to power future Internet of Things-related applications."

The DesignWare AEON MTP ULP NVM IP offers single-bit read capability to give designers additional flexibility in setting power/timing tradeoffs, which can depend on the peak current and read time requirements. To reduce factory programming test costs, the IP includes a fast programming mode that cuts programming time by 70 percent compared to the previous generation. With up to 100,000 write cycle endurance, RFID and NFC designers using DesignWare AEON MTP ULP NVM IP can have confidence that their products can be reprogrammed many times for extensive reuse. In addition, the IP integrates critical high-voltage generation and distribution circuitry to simplify integration and reduce system cost and area.

"To achieve their systems' power and cost objectives, designers in the competitive wireless and RFID/NFC tag markets need the lowest power and smallest area NVM IP for their ICs," said John Koeter, vice president of marketing for IP and systems at Synopsys. "Synopsys DesignWare NVM IP, the industry's broadest portfolio of CMOS MTP IP, has shipped in well over three billion chips and over 40 process nodes. With the new DesignWare AEON MTP ULP NVM IP, Synopsys is building on its years of NVM technology leadership to deliver proven IP that lowers integration risk and speeds time to market."

Availability

DesignWare AEON MTP ULP NVM IP is available now in the 180 nanometer process node.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To

support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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