Synopsys and CEVA Deliver Superior Performance, Power and Area for CEVA DSP Cores with DesignWare HPC Design Kit

HPC Design Kit of Optimized Embedded Memories and Logic Libraries Yields 8 Percent Performance Improvement and 13 Percent Leakage Power Reduction with Smaller Area for CEVA-XC DSPs

MOUNTAIN VIEW, Calif., Nov. 12, 2013 /PRNewswire/ --

Highlights:

- CEVA and Synopsys collaborated to develop highly optimized DSP core implementations for wireless communications applications including base stations and handsets
- Results enabled by Synopsys' DesignWare HPC Design Kit, a processor optimization kit that includes more than 125 standard cells and memory instances, and an ultra-high density memory compiler
- CEVA achieved an 8 percent performance improvement (worst-case operating conditions) over previous results, and a maximum performance of 1.3 GHz in a 28-nm process while also achieving area and power targets for base-station applications
- Collaboration reduced leakage power by 13 percent and total power by 10 percent while also achieving speed targets for handset applications

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems and CEVA, Inc. (NASDAQ: CEVA), the leading licensor of silicon intellectual property (SIP) DSP cores and platform solutions, today announced that the collaboration between the two companies has resulted in highly optimized implementations of the CEVA-XC DSP cores targeting the high-performance needs of base-station applications and the low-power requirements of handset applications. CEVA used Synopsys' DesignWare® High Performance Core (HPC) Design Kit to optimize its DSP for performance, power and area, achieving an 8 percent improvement in performance at 1.3 GHz maximum operating frequency for its base-station application and reducing leakage power by up to 13 percent for its handset application, compared to previous implementations in the same technology. The DesignWare HPC Design Kit is a suite of optimized high-speed and high-density memories and logic libraries that allow system-on-chip (SoC) designers to optimize their processor cores for maximum speed, smallest area, lowest power, or for an optimum balance of the three for their specific application.

"DSPs are a key technology for today's fastest growing wireless and consumer electronic applications, and at CEVA we endeavor to meet our customers' design goals with DSPs optimized for power, performance and area to address their specific requirements," said Eran Briman, vice president of marketing at CEVA. "Our successful collaboration with Synopsys using their DesignWare HPC Design Kit has yielded impressive improvements in the performance and power of our CEVA-XC DSP cores, and is indicative of the efficiencies that this optimization process is capable of delivering across our portfolio of DSPs."

The CEVA-XC DSP architecture features a combination of VLIW (Very Long Instruction Word) and Vector engines that enhances typical DSP capabilities with advanced vector processing. The scalable CEVA-XC architecture offers a selection of highly powerful communication processors, with four generations to date (CEVA-XC321™, CEVA-XC323™, CEVA-XC4210™ and CEVA-XC4500™) widely licensed by leading vendors with over 20 design wins to date. The CEVA-XC architecture targets a broad range of communication applications and use cases including LTE-Advanced handsets, wireless infrastructure, Wi-Fi stations and access points, cable modem, satellite modem and more.

Synopsys' DesignWare HPC Design Kit is an add-on to the DesignWare Duet package of embedded memories and logic libraries. The Duet package contains all the physical IP elements needed to implement a complete SoC including standard cells, SRAM compilers, register files, ROMs, datapath libraries and Power Optimization Kits (POKs), as well as options for overdrive/low voltage process, voltage and temperature corners (PVTs), multi-channel cells and memory built-in self-test (BIST) and repair. The HPC Design Kit adds fast cache memory instances and performance-tuned flip-flops that enable speed improvement for processor cores of up to 10 percent over the standard Duet package. To minimize dynamic and leakage power as well as die area, the HPC design kit provides area-optimized and multi-bit flip-flops as well as an ultra-high density two-port register file, which reduces area and power by up to 25 percent while maintaining processor performance. Optimized design flow scripts and expert core implementation consulting services are also available to help design teams achieve their processor and SoC design goals in the shortest possible time.

"Physical IP elements including embedded memories and standard cell libraries are central to achieving the best performance, power and area results for DSP cores," said John Koeter, vice president of marketing for IP

and systems at Synopsys. "Our successful collaboration with CEVA to optimize their CEVA-XC DSP cores using Synopsys' DesignWare HPC Design Kit has resulted in substantial gains across the full speed, power and area spectrum, enabling designers to meet the design requirements of their target application."

Availability

- The Synopsys DesignWare HPC Design Kit is available from Synopsys now
- The CEVA-XC Family of DSPs are available from CEVA now

About CEVA, Inc.

CEVA is the world's leading licensor of silicon intellectual property (SIP) DSP cores and platform solutions for the mobile, portable and consumer electronics markets. CEVA's IP portfolio includes comprehensive technologies for cellular baseband (2G / 3G / 4G), multimedia (vision, imaging and HD audio), voice processing, Bluetooth, Serial Attached SCSI (SAS) and Serial ATA (SATA). In 2012, CEVA's IP was shipped in over 1.1 billion devices, powering smartphones from many of the world's leading OEMs, including HTC, Huawei, LG, Nokia, Motorola, Samsung, Sony, TCL and ZTE. Today, more than 40% of handsets shipped worldwide are powered by a CEVA DSP core. For more information, visit www.ceva-dsp.com. Follow CEVA on twitter at www.twitter.com/cevadsp.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

Editorial Contacts:

Monica Marmie
Synopsys, Inc.
650-584-2890
monical@synopsys.com

Richard Kingston
CEVA, Inc.
650-417-7976
info@ceva-dsp.com

Stephen Brennan
MCA, Inc.
650-968-8900, ext.114
sbrennan@mcapr.com

SOURCE Synopsys, Inc.