Synopsys Announces DesignWare ARC HS Processors for Next-Generation Embedded Data and Signal Processing Systems

New Performance-Efficient Design Optimized for Maximum DMIPS/mm2 and DMIPS/milliwatt

MOUNTAIN VIEW, Calif., Nov. 5, 2013 /PRNewswire/ --

Highlights:

- DesignWare ARC HS34 and HS36 cores are the first members in a new family of high-speed, low-power processors based on the extensible ARCv2 architecture
- New 32-bit cores deliver more than 4200 DMIPS while consuming less than 85 milliwatts of power and only 0.15 mm^2 of silicon area in typical 28-nm processes
- High degree of configurability enables users to tailor the cores for their specific embedded applications such as connected appliances, automotive, SSDs and home networking
- Custom instructions let designers integrate proprietary hardware accelerators into the processor to optimize overall system performance and reduce memory size
- Open architecture supports close coupling of memory and direct-mapped peripherals to minimize system latency while reducing power and silicon area
- Broad ecosystem of software development tools, operating systems and middleware from Synopsys and third-party partners accelerate the design of ARC-based systems

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced availability of the first products in the new DesignWare® ARC® HS Processor Family. The 32-bit ARC HS34 and HS36 processors are the highest performance ARC processor cores to date, delivering 1.9 DMIPS/MHz at speeds up to 2.2 GHz in typical 28-nanometer (nm) silicon. The new HS processors are optimized for power efficiency (DMIPS/mW) and area efficiency (DMIPS/mm^2) while performing high speed data and signal processing tasks. This optimization makes them ideally suited for the embedded and deeply embedded processors within system-on-chips (SoCs) for products such as solid-state drives, connected appliances, automotive controllers, media players, digital TV, set-top boxes and home networking products.

"To keep pace with evolving market requirements in the digital TV market, our design teams are under constant pressure to deliver higher performance at lower power and cost points," said Yves Mathys, CEO at Abilis Systems. "Synopsys' ARC HS processors will enable us to achieve new levels of high performance and low power in our embedded designs with significant chip area savings. Leveraging ARC hardware and software development tools and third-party support will also help us keep our design schedules on track, which is critical as we introduce new digital media products."

Scalable Performance

The new ARC HS Processor Family utilizes the next-generation ARCv2 instruction-set architecture (ISA), which enables the implementation of high performance embedded and deeply embedded designs with ultra-low power consumption and a very compact silicon footprint. When implemented in typical 28-nm processes, the HS cores consume as little as 0.025mW/MHz in an area as small as 0.15mm^2. The cores feature a high-speed 10-stage pipeline that supports out-of-order execution, minimizing idle processor cycles and maximizing instruction throughput. Sophisticated branch prediction and a late-stage ALU improve the efficiency of instruction processing. To speed the execution of math functions, the ARC HS Processors give designers the option to implement a hardware integer divider, instructions for 64-bit multiply, multiply-accumulate (MAC), vector addition and vector subtraction, and a configurable IEEE 754-compliant floating point unit (single- or double-precision or both). The ARCv2-based cores provide an 18 percent improvement in code density compared to previous generation ARC cores, reducing memory requirements. HS processors also support close coupled memory as well as instruction and data cache (HS36 only), with new 64-bit load-double/store-double and unaligned memory access capabilities that accelerate data transfers. Optional error-correcting code (ECC) hardware is available for all memories in the processor for applications that require a higher level of memory reliability and protection.

"Designing processors for high performance is simple when power and transistor budgets are not a concern. Much more difficult is designing small, efficient processors that offer enough performance for today plus

additional headroom for future growth," said Linley Gwennap, principal analyst of The Linley Group. "To optimize their ARC HS cores for embedded applications, Synopsys took a more streamlined approach, using fewer transistors and less power yet still delivering high throughput with an unusually flexible CPU that SoC designers can customize extensively. Its strong power efficiency and low-cost silicon footprint will appeal to many embedded-system developers."

Configurability and Extensibility

The highly-configurable ARC HS processors allow designers to tailor each instance of the core on their SoC for the optimum balance of performance, power and area. Users can define instruction extensions to the processor pipeline that enable the integration of their own proprietary hardware accelerators that can dramatically improve application-specific performance while reducing power consumption and the amount of memory required. Native ARM® AMBA® AXI™ and AHB™ standard interfaces are configurable for 32-bit or 64-bit transactions to optimize system throughput. SoC peripherals can be directly accessed by the CPU in a single cycle, minimizing system-level latencies and maximizing hardware integration. By incorporating features to optimize the performance efficiency of both the processor and the system, the HS34 and H36 cores give designers the ability to create greater product differentiation while lowering the cost of implementation.

Robust Software Development Support

The new HS cores are supported by the Synopsys MetaWare Development Kit, a complete solution for developing, debugging, and optimizing embedded software on ARC processors. The kit includes an optimized compiler to generate highly efficient code, a debugger for maximum visibility into the software and a fast instruction set simulator (ISS) for pre-hardware software development. A 100 percent cycle-accurate simulator is also available for design optimization and verification. Operating system (OS) support for the HS Processor Family includes Synopsys' MQX RTOS, a full-featured real-time operating system optimized for deterministic response times and memory size efficiency. Additional third-party hardware and software tools supporting software development on ARC HS processors are available from ARC Access Program partners include advanced debugging tools from Ashling Microsystems and Lauterbach and the popular ThreadX RTOS from Express Logic.

"With more than 1.3 billion ARC-based chips shipping annually, we are keenly aware that each new generation of electronic devices requires processors to meet the conflicting goals of higher performance with lower power and smaller area, and that's exactly what the ARC HS Processor Family delivers," said John Koeter, vice president of marketing for IP and systems at Synopsys. "The ARC HS34 and HS36 cores represent a significant advancement in the ARC portfolio and demonstrate Synopsys' commitment to extending the ARC roadmap to meet designers' evolving embedded requirements."

Availability & Resources

The DesignWare ARC HS34 and ARC HS36 processor cores and associated development tools are available immediately. For more information, visit: http://www.synopsys.com/arc.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the

world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

Editorial Contacts:
Monica Marmie
Synopsys, Inc.
650-584-2890
monical@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900, ext.114
sbrennan@mcapr.com

SOURCE Synopsys, Inc.