Synopsys Extends Performance Exploration Solution for ARM AMBA 4 Interconnect-based Multicore SoCs

Platform Architect with New SystemC Model for ARM CoreLink NIC-400 Network Interconnect Enables Optimization of SoC Performance from among Thousands of Configurations

MOUNTAIN VIEW, Calif., Oct. 30, 2013 /PRNewswire/ --

Highlights:

- Exploration of ARM CoreLink NIC-400 performance parameters with instrumentation for simulation and analysis easily identifies performance bottlenecks
- Enables fast transaction-level simulation, with fully cycle-accurate model validated against the ARM® CoreLink™ NIC-400 RTL
- Efficient hand-off to RTL implementation by sharing the optimal interconnect configuration with ARM AMBA® Designer tool
- Seamless sharing of system-level performance constraints with Synopsys' Discovery™ Verification IP platform ensures consistency of performance requirements specification through functional verification

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the extension of its Platform Architect™ with multicore optimization (MCO) technology performance exploration solution for ARM AMBA 4 interconnect-based SoCs to support ARM CoreLink NIC-400 network interconnect-based designs. Synopsys Platform Architect MCO and Synopsys' new SBL-400 SystemC model of the ARM CoreLink NIC-400 network interconnect enable SoC architects to efficiently explore thousands of system configurations, visualize the impact that interconnect and memory subsystem parameters have on system performance, power, and cost, and identify the optimum combination for their SoC design early in the development process.

"Architecture simulation is important for the successful development of multicore image processing SoCs and helps us optimize system performance and cost," said Hirohisa Kotegawa, director of system level design & verification department, SoC design center business unit at Fujitsu Semiconductor Limited (FSL). "With Synopsys Platform Architect MCO and the ARM AMBA Designer, we can combine transaction-level models of FSL image processing IP with accurate interconnect models from Synopsys to analyze performance, make architecture decisions earlier that improve the logic design, and be more confident that interconnect and memory subsystem performance will meet specification. As users of the SBL-301 model from Synopsys, we are pleased to see the extension of this solution to support ARM CoreLink NIC-400 interconnect and the AMBA Designer flow."

Using Synopsys' Platform Architect MCO and SBL-400 model, system designers can explore NIC-400 configuration parameters at run-time, enabling efficient simulation sweeping, data collection, sensitivity analysis, root cause analysis, and performance and cost optimization from thousands of configurations. The integration of Platform Architect MCO with the AMBA Designer tool efficiently manages the configuration information for system-level exploration, and uses the configuration checks in AMBA Designer to validate the candidate architecture. The tool saves the optimal configuration in a file for the hardware team to use and extend in AMBA Designer with the information required for RTL implementation.

"Designers of ARM CoreLink NIC-400-based SoCs want to maximize their system performance by choosing an optimal interconnect configuration that combines the necessary quality-of-service with the lowest power consumption and at a low cost," said Andy Nightingale, director, System IP products, Processor Division at ARM. "Synopsys Platform Architect MCO and the SBL-400 model, integrated with ARM AMBA Designer and Synopsys Discovery Verification IP, deliver a complete solution for the optimization and validation of these multicore SoCs."

Platform Architect also generates performance constraint information for the optimal design that is easily reused to configure the performance monitors of Synopsys Discovery Verification IP (VIP) for AMBA interconnect. This enables RTL verification teams to validate the performance of the architecture while doing functional verification, thereby uncovering hidden performance issues and avoiding delays from late architectural changes that would otherwise impact system-level performance. By using Discovery VIP, verification teams can easily check performance constraints—with practically zero additional effort. Verification engineers can focus on ensuring that the design adheres to the system specification, including performance and protocol correctness, as they add IP blocks to the design.

"To maximize return on investment, project teams developing multicore SoCs must identify architecture problems as early as possible," said John Koeter, vice president of marketing for IP and systems at Synopsys. "Platform Architect's exploration, performance optimization and system validation capabilities enable architects to visualize key architecture trade-offs very early

in the development process, helping to avoid design mistakes and costly SoC re-work late in the development process."

Availability & Resources
Platform Architect with multicore optimization technology is available now with support for ARM AMBA 2, AMBA 3, and AMBA 4 protocols, including AXI4 and ACE. Synopsys' new SBL-400 SystemC model of the ARM CoreLink NIC-400 network interconnect will be generally available in December, 2013. This includes Synopsys' distribution and support of ARM AMBA Designer ESL for use with Synopsys' SBL-400 and SBL-301 models of ARM CoreLink interconnect.

- Learn more about Platform Architect at: http://www.synopsys.com/PlatformArchitect

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Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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