Synopsys Announces Availability of Discovery Verification IP for ARM AMBA 5 CHI Standard

Discovery VIP Successfully Leveraged by Early Licensees Now Broadly Available

MOUNTAIN VIEW, Calif, Oct. 28, 2013 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of its Discovery™ Verification IP (VIP) for the ARM® AMBA® 5 CHI (Coherent Hub Interface) on-chip interface specification. This standard targets the ARM Cortex®-A50 series processors used in high data rate applications common in enterprise markets such as the server and networking markets. The Synopsys Discovery VIP for AMBA 5 CHI provides an easy-to-use, high-performance verification environment with unique protocol-aware debug capabilities and advanced built-in coverage features designed to accelerate the system-on-chip (SoC) verification closure process.

"Our networking QorIQ SoCs with the revolutionary new Layerscape architecture are designed to enable hundreds Gb/s performance and enhanced packet processing capabilities," said Fares Bagh, vice president of Hardware Engineering for Freescale's Digital Networking business. "Developing the design environment for such SoC complexity required a complete verification framework with a single-testbench and debug methodology from simulation all the way to emulation. As an early collaborator, the deployment of the Synopsys Discovery VIP for ARM AMBA 5 CHI was a critical element to this verification framework as we look to leverage its 100% SystemVerilog, UVM-based VIP architecture across all interface and on-chip bus protocols."

"Since its introduction earlier this year, the AMBA 5 CHI protocol has been deployed in several key SoCs to deliver optimal system operation, especially for high-performance applications," said Andy Nightingale, director of System IP, ARM. "These complex SoCs in turn offer challenging verification requirements. Through our early collaboration, Synopsys' verification IP equips SoC teams with verification, debug and performance analysis technology to accelerate the development of AMBA 5 CHI-based SoCs."

"ARM and Synopsys have a 15-year history of successful R&D collaboration to deliver verification solutions, including SystemVerilog, verification methodology, simulation performance, low power verification, debug, interface IP and, most recently, our verification IP for AMBA 5 CHI interconnect," said Debashis Chowdhury, vice president of R&D in the Synopsys Verification Group. "Through this collaboration, Synopsys continues to deliver advanced verification technology for simulation, emulation, debug and performance analysis to speed the design of advanced ARM-based SoCs."

On October 30, 2013 at 2:30 p.m. PDT, Synopsys will be hosting a live session at the ARM TechCon Conference on "AMBA 5 CHI verification using Discovery Verification IP." Registration is now open at http://schedule.armtechcon.com/session-id/150.

On November 20, 2013 at 10:00 a.m. PST, Synopsys will be hosting a webinar, "Meeting the Challenge of Verifying ARM AMBA 5 CHI Interconnect-Based SoCs Using Next-Generation VIP." Click here to register for the webinar.

About Discovery Verification IP

Discovery VIP, based on Synopsys' next-generation VIPER architecture and implemented in 100 percent SystemVerilog, offers enhanced VIP ease-of-use, configurability, performance, debug, coverage and extensibility. Discovery VIP supports Synopsys' Protocol Analyzer, a protocol-centric debug environment with intelligent visibility into the VIP source code. These capabilities substantially increase user productivity for one of the most difficult and time-consuming aspects of SoC design and verification. For more information, visit www.synopsys.com/vip.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 x115
lgmartin@mcapr.com

SOURCE Synopsys, Inc.