Synopsys Extends DesignWare IP Portfolio for Data Center SoCs with Enterprise 40G Ethernet Controller IP

DesignWare IP Optimized to Address Throughput and Quality-of-Service Requirements in Modern Data Center SoCs

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Highlights:

- Synopsys DesignWare® Enterprise 40G Ethernet MAC and PCS Controller IP optimized for high performance and energy efficiency to address data center system throughput and quality-of-service requirements
- Synopsys' complete 40G Ethernet IP solution includes DesignWare Enterprise 40G Ethernet Controller IP, Enterprise 10G PHY and Verification IP
- Supports 1G, 2.5G, 10G and 40G network speeds, giving enterprise application designers the ability to easily migrate designs to faster data rates
- Supports latest IEEE 802.3 specifications for Ethernet-based LANs to simplify integration and reduce interoperability risk
- Part of the DesignWare data center IP portfolio, which includes solutions for 1G/10G Ethernet, DDR4/3, PCI Express® 3.0/2.0, USB 3.0/2.0, SATA 6G and the ARM® AMBA® AXI4™ and AMBA 3 interconnect; logic libraries and embedded memories; and Synopsys ARC® processors
- Energy-Efficient Ethernet and Wake-on-LAN features reduce power consumption in power-hungry data centers

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of the DesignWare Enterprise 40G Ethernet MAC and PCS Controller IP as part of Synopsys' complete Enterprise 40G IP solution. The rise of "mega data centers" comes with significant pressure to reduce their size, power consumption and cost of operation. With support for Energy-Efficient Ethernet (EEE) and Wake-on-LAN, the DesignWare Enterprise 40G Controller IP enables system architects to meet low power and low latency requirements for data center applications, including software-defined networking (SDN) and low-power micro servers. In addition, the DesignWare Enterprise 40G Ethernet MAC and PCS Controller IP are compliant with the IEEE 802.3ba specification in IEEE 802.3-2012, enabling designers to configure and implement the IP in their SoCs with less risk and improved interoperability.

"Due to the focus on improved power efficiency in data centers, transmitting enormous amounts of data over Ethernet networks requires more high-speed I/Os and CPU cores per chip to optimize performance per watt," said Jag Bolaria, senior analyst at the Linley Group. "Next-generation server-on-a-chip designs are combining external system logic and interfaces such as 40G Ethernet, DDR3L/DDR4 SDRAMs, PCI Express and SATA to reduce server size and power. This new wave of servers-on-chips will be enabled by third-party IP providers such Synopsys, who provide a broad range of IP for these applications."

With the growth in power-hungry enterprise server applications, support for low-power features is a key differentiator in data center SoCs. The DesignWare Enterprise 40G Ethernet Controller IP reduces power consumption by incorporating the Wake-on-LAN feature, which detects LAN wake-up frames and magic packet frames in power-down mode. This feature, used in conjunction with the system's existing power-down modes, allows designers to enable/disable functions as needed. Standard interfaces support easy PHY integration for 1G to 40G speeds so designers can select the data rate they need for their current project, with a clear path to higher speeds for future designs.

In addition to incorporating the Wake-on-LAN feature, DesignWare Enterprise 40G Controller IP supports the IEEE 802.3az specification for Energy-Efficient Ethernet (EEE) to further reduce power consumption during periods of low link utilization. The EEE standard takes advantage of systems' idle times to reduce power consumption by up to 50 percent while maintaining compatibility with existing equipment. Reducing power consumption is not only an energy-saving opportunity, but also enables higher port density, lowering costs for end users.

The DesignWare Enterprise 40G Controller IP is part of Synopsys' data center IP portfolio, which includes IP for 1G/10G/40G Ethernet, DDR4/3, PCI Express 3.0/2.0, USB 3.0/2.0, SATA 6G and the ARM AMBA AXI4 and AMBA 3 interconnect; logic libraries and embedded memories; and ARC processors. The portfolio incorporates key data center features such as low latency, low power, multi-port memory, I/O virtualization, data center bridging, FIS-based switching, TCP segment offload and Energy-Efficient Ethernet. By providing the IP needed for data center SoCs, Synopsys enables designers to work with a single, trusted IP provider to lower integration risk and achieve their design goals faster.

"As a leading provider of Ethernet IP with more than 450 Ethernet IP design wins, Synopsys continues to deliver high-quality Ethernet IP solutions that incorporate the necessary power, performance and latency features required for today's advanced SoCs in data center applications," said John Koeter, vice president of marketing for IP and systems at Synopsys. "The addition of the DesignWare Enterprise 40G Ethernet Controller IP to Synopsys' comprehensive IP portfolio for data centers helps

designers quickly deploy innovative networking and server SoCs to the market, enabling the growth of next-generation cloud computing."

Availability

DesignWare Enterprise 40G Ethernet PCS and MAC Controller IP are available now. In addition, the IP for data center applications, including IP for 1G/10G Ethernet, DDR4/3, PCI Express 3.0/2.0, USB 3.0/2.0, SATA 6G and the ARM AMBA AXI4 and AMBA 3 interconnect; logic libraries and embedded memories; and ARC processors are all available now.

For additional information:

- Register for the "Enterprise Ethernet IP for Data Center SoC Design" webinar
- Learn more about DesignWare Enterprise 40G Ethernet Controller IP

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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