Synopsys Introduces DesignWare ARC EM SEP Processor for Safety-Compliant Automotive Systems

Integrated Safety Features and ASIL D Ready Compiler Ease Development of ISO 26262-Compliant SoC Designs

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Highlights:

- Optimized for high-efficiency, low-power embedded automotive applications
- Automotive Safety Integrity Level D (ASIL D)-ready DesignWare ARC MetaWare Compiler streamlines development of ISO 26262-compliant software
- Integrated safety features include parity support and error-correcting code (ECC) technology
- Detailed IP safety documentation eases certification of ARC EM SEP-based systems

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced availability of the new DesignWare® ARC® EM SEP (Safety Enhancement Package) Processor core for automotive safety-compliant applications. The 32-bit ARC EM SEP processor is based on the highly efficient ARC EM4 core. It delivers performance up to 300 MHz and power consumption as low as 16 mW/MHz on typical 65-nanometer (nm) low power silicon processes, with integrated hardware safety features that enable ASIL D compliance in support of the ISO 26262 standard. In addition, the DesignWare ARC MetaWare Compiler helps software developers accelerate the development of ISO 26262-compliant code and is undergoing ASIL D readiness certification by SGS-TUV Saar, a leading independent safety certification company. The combination of a safety-enhanced processor and compiler makes the ARC EM SEP core ideally suited for system-on-chips (SoCs) designed for embedded automotive applications such as movement and acceleration sensors, advanced driver assistance systems and electric power steering.

"As a provider of high-performance semiconductors for use in automotive systems it is critical that our products adhere to the highest safety standards," said Vijay Mangtani, business unit director for power ICs at Allegro MicroSystems. "Support for ISO 26262 automotive safety standards is key to enabling us to meet automotive safety system requirements in our chips. Synopsys' commitment to support these standards in processor cores like the ARC EM SEP helps automotive IC designers meet this important market requirement."

The ARC EM SEP core is configurable to meet the unique performance, power and area requirements of each target application. Giving designers the ability to define custom instructions facilitates the integration of proprietary hardware accelerators that improve application-specific performance while reducing power consumption and the amount of memory required—critical requirements in embedded automotive designs. The EM SEP processor integrates hardware safety features including ECC for single-bit error correction and double-bit error detection, and parity protection for single-bit error detection on closely coupled memories. To minimize system-level latencies and silicon area, SoC peripherals can be directly mapped to the CPU to enable single cycle access. Native ARM® AMBA®, AHB™, AHB-Lite™ and BVCI standard interfaces are configurable for 32-bit or 64-bit transactions to optimize system throughput. Support for ARC EM SEP in Synopsys' Virtualizer™ virtual prototyping environment allows for seamless integration with tools such as Mathworks' Simulink®, Vector's CANoe and Synopsys' Saber to enable virtual hardware-in-the-loop (HIL) simulation and fault testing.

The DesignWare ARC MetaWare Compiler and accompanying safety documentation help developers of

safety-critical systems fulfill the requirements of the ISO 26262 standard. The IP safety collateral, including a safety manual and safety guide, makes it easier for automotive designers to prepare their documentation for ISO 26262 compliance testing. The compiler is part of the ARC MetaWare Development Toolkit, a complete solution for developing, debugging and optimizing embedded software targeted for ARC processors.

"Today, most critical functions in vehicles are heavily managed by electronics, driving the need for IP that has integrated safety features that meet automotive safety standards," said John Koeter, vice president of marketing for IP and systems at Synopsys. "Synopsys' new DesignWare ARC EM SEP processor and ASIL D ready compiler save designers of automotive electronic chips and systems time and effort on their path to ISO 26262 certification."

Availability & Resources

General availability of the DesignWare ARC EM SEP processor core, certified ASIL D ready compiler and associated development tools is planned for the end of October, 2013. For more information, visit: http://www.synopsys.com/arc.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected availability of Synopsys' DesignWare ARC EM SEP processor core. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen production or delivery delays, failure to perform as expected, product errors or defects and other risks as identified in Synopsys' filings with the Securities and Exchange Commission, including those described in the "Risk Factors" section of Synopsys' latest Quarterly Report on Form 10-Q.

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