TSMC Awards Synopsys "Partner of the Year 2013" for Joint Development of 16-nm FinFET Design Infrastructure

Synopsys Recognized for Valuable Contributions Towards Development of FinFET Technology

MOUNTAIN VIEW, Calif., Oct. 14, 2013 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that TSMC awarded Synopsys its Open Innovation Platform "Partner of the Year 2013" for joint development of 16-nanometer (nm) FinFET design infrastructure. The award recognizes Synopsys' broad and deep technical expertise and shared commitment to the development and delivery of TSMC's 16-nm Reference Flow, validated on a quad-core ARM® Cortex™-A15 mobile processor design. The design infrastructure solution from Synopsys includes the Design Compiler®, IC Compiler™, StarRC™, PrimeTime® and IC Validator tools.

"Synopsys has made significant contributions with foundational technologies, including parasitic extraction, to make FinFET seamless for mutual customers," said Suk Lee, TSMC Senior Director of Design Infrastructure Marketing Division. "We are pleased to present the Partner of the Year 2013 award to Synopsys and look forward to enabling our customers to deliver innovative designs that run fast and consume less power."

"We are honored to receive this prestigious award from TSMC," said Bijan Kiani, vice president of product marketing at Synopsys. "The complexity of FinFET technology demands close collaboration amongst semiconductor ecosystem partners. The strong engineering collaboration with TSMC on the 16nm FinFET process enables us to collectively advance the state-of-the-art for design engineers."

About Synopsys Support for the TSMC 16-nm Reference Flow

Synopsys' Galaxy Implementation Platform provides tools and methodology support for TSMC's 16-nm Reference Flow:

- Design Compiler: Advanced optimization technologies including placement, congestion and layer awareness for superior results
- IC Compiler: Advanced technology supports 16 nm FinFET quantized rules, FinFET grid rules and advanced optimization methodology including PBA vs GBA timing correlation and low voltage analysis to achieve optimal performance, power and area
- IC Validator: DRC and DPT rule compliance check verifying FinFET parameters including fin boundary rules and expanding dummy cells
- PrimeTime: Advanced waveform-propagation delay calculation delivers STA signoff accuracy required for FinFET processes
- StarRC: FinFET device modeling with real profile provides precise middle-end-of-line (MEOL) parasitic extraction for accurate transistor-level analysis

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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