Synopsys and TSMC Collaborate to Deliver 16-nm Custom Design Reference Flow

TSMC Includes Analog/Mixed-Signal Products for 16-nm Design Requirements

MOUNTAIN VIEW, Calif., Oct. 14, 2013 /PRNewswire/ --

Highlights:

- HSPICE, Laker, and IC Validator enhanced to support voltage-dependent design rules (VDRC) from simulation through signoff verification
- Laker custom design solution ready for TSMC 16-nm FinFET process requirements
- HSPICE, CustomSim and FineSim bring accuracy for latest FinFET modeling standard
- CustomSim included for electromigration and IR-drop analysis

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that it has collaborated with TSMC to provide support for voltage-dependent design rules in TSMC's 16-nm Custom Design Reference Flow. As part of TSMC's custom design infrastructure, TSMC has also certified Synopsys' Laker® custom design solution and circuit simulation tools that deliver new capabilities for TSMC V0.5 16-nm FinFET process layout design rules, device models, and electromigration and IR-drop (EM/IR) analysis. TSMC and Synopsys will continue to collaborate on certification of the Synopsys tool set until 16nm FinFET reaches V1.0.

"TSMC works with Synopsys to ensure our customers have access to analog and mixed-signal design tools for TSMC's 16-nanometer FinFET process," said Suk Lee, senior director of design infrastructure marketing at TSMC. "The Custom Design Reference Flow is another milestone of the long term collaboration between the two companies."

"Synopsys continues to build on our strengths in custom design," saidBijan Kiani, vice president of product marketing at Synopsys. "Designers rely on us to provide circuit simulation and RC extraction, and are increasingly looking to us as their complete custom design solution provider, particularly with the move to 16-nanometer process technologies."

Voltage-dependent Design Rules

For the TSMC Custom Design Reference Flow, Synopsys' HSPICE® circuit simulation, Laker custom layout and IC Validator physical implementation tools have been brought together to provide a comprehensive solution for voltage-dependent design rule checking. VDRC rules require larger spacing between signals that have a high potential voltage difference. For VDRC validation, voltage ranges are calculated for each net by HSPICE circuit simulation, annotated onto the layout by the Laker layout editor, and then verified using IC Validator signoff verification.

Laker Custom Design Solution Updates

Laker enhancements for 16-nm layout include an extensive set of new features for FinFET devices, including fin grid pattern snapping, fin display and interactive FinFET rule checking. Laker's built-in double-pattern checking has been enhanced to support pre-coloring and color density checking. Laker support for middle end-of-line (MEOL) layers includes contactless connectivity, unidirectional layer rules and enhancements to support 16-nm guard rings.

Circuit Simulation Performance and Accuracy

Synopsys has optimized the FinFET model used in HSPICE, CustomSim™ and FineSim® for better performance, reduced memory footprint and enhanced multi-threading scalability. The TSMC Modeling Interface (TMI2.0) jointly developed by TSMC and Synopsys enables more accurate layout-dependent effect modeling on top of standard SPICE models. TMI2.0 also provides a unified infrastructure for statistical modeling, and MOS aging simulation.

IC Validator Signoff Physical Verification for16-nm FinFET

Synopsys has collaborated with TSMC to provide full signoff-accurate runsets for design rule checking (DRC) and layout-vs.-schematic (LVS) checks with TSMC 16-nm V0.5. IC Validator is also integrated into the Laker user environment to allow running DRC and LVS signoff checks and for debugging layout errors with IC Validator's VUE utility.

Electromigration and IR-drop Analysis

Low power design techniques in 16-nm designs require accurate, simulation-based EM/IR analyses. Through close

collaboration with TMSC, Synopsys has enhanced its CustomSim EM/IR analysis capability to comply with the new rules for 16-nm designs and support TSMC's iRCX format.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

Editorial Contacts:
Monica Marmie
Synopsys, Inc.
650-584-2890
monical@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

SOURCE Synopsys, Inc.