Synopsys Implementation Solution Included in TSMC 16-nm Reference Flow for FinFET Design

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Highlights:

- Multi-year collaboration delivers proven 16-nm design flow and methodology
- Synopsys tools are under V0.5 certification and moving forward to V1.0 for FinFET solutions in extraction, P&R, custom design, physical verification, STA, circuit simulation and power rail integrity analysis
- 16-nm FinFET Reference Flow solution deployed for early adopters of TSMC 16-nm FinFET process

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced delivery of a comprehensive design implementation solution for TSMC's 16-nanometer (nm) FinFET reference flow. The jointly developed reference flow is built on tool certification currently in TSMC's V0.5 Design Rule Manual (DRM) and SPICE. TSMC and Synopsys will continue to collaborate on tool sets for 16-nm FinFET V1.0 certification. The collaboration covers device modeling and parasitic extraction, place and route (P&R), custom design, static timing analysis (STA), circuit simulation, rail analysis, and physical and transistor verification technologies included in Synopsys' Galaxy™ Implementation Platform. SoC design teams can use the silicon-proven, project-ready solution to implement FinFET-based designs, and together with the reference flow, early adopters of the TSMC 16-nm process will realize the potential of FinFET technology to develop faster, more power-efficient designs.

"TSMC has collaborated with Synopsys on methodology innovation and tool integration for 16nm FinFET technology," said Suk Lee, TSMC Senior Director, Design Infrastructure Marketing Division. "Our long-standing collaboration covers the design implementation flow and helps early adopters access our advanced processes and accelerate the deployment of FinFET technology."

"Our collaboration with TSMC has resulted in a comprehensive FinFET implementation flow that can be deployed for production use by our mutual customers," said Bijan Kiani, vice president of product marketing, design & manufacturing products at Synopsys. "The Galaxy flow enables transparent adoption of FinFET technology so designers can seamlessly take advantage of the performance and power benefits of this advanced process geometry."

TSMC's release of this comprehensive implementation solution enables adopters of the TSMC 16nm Reference Flow to fully realize the technology advantages in power, performance, area and manufacturability.

Synopsys' Galaxy Implementation Platform provides tools and methodology support for TSMC's 16-nm Reference Flow:

- IC Compiler: Advanced technology supports 16nm FinFET quantized rules, FinFET grid rules and advanced optimization methodology including PBA vs GBA timing correlation and low voltage analysis to achieve optimal performance, power and area
- IC Validator: DRC and DPT rule compliance check verifying FinFET parameters including fin boundary rules and expanding dummy cells
- PrimeTime®: Advanced waveform-propagation delay calculation delivers golden STA signoff accuracy required for FinFET processes
- StarRC™: Pioneering "real profile," FinFET device modeling provides the most precise middle-end-of-line (MEOL) parasitic extraction for accurate transistor-level analysis

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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